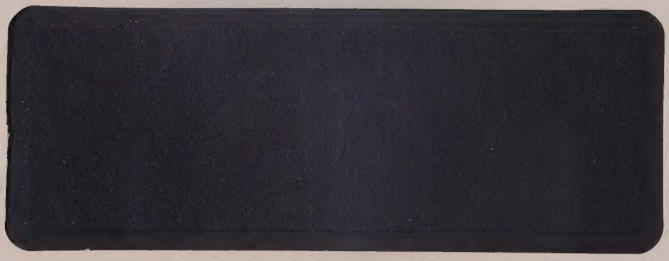
Operator's Manual

MODEL TR8828 SERIES
AND MM8103A, MM8104, MM8105
WAVEFORM RECORDING SYSTEM

LeCroy

Innovators in Instrumentation



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WAVEFORM RECORDING SYSTEM

MASTER COPY

March 1987

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Innovators in Instrumentation

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CAUTION

COOLING

The high power dissipation of the TR8828 requires that it be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature to less than 50° C. Do not install module in furthest left slot of crate, as cooling is often less sufficient there.

TERMINATION RESISTORS

Proper installation of the memory modules requires removal of resistor terminators from all memories except the one furthest from the TR8828 Series. See Chapter 3.

BATTERY

Unsolder one lead of the battery or remove jumper E1–E2 before attempting repairs on these modules.

INSTALLATION

Crate power should be turned off during insertion or removal of module to avoid possible damage caused by momentary misalignment of contacts.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

1 GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation, packaged separately, should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in–warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Services Department, 700 South Main Street, Spring Valley, New York 10977, (914) 425–6059, or your local field service office.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on–site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state–of–the–art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up–to–date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

2 PRODUCT DESCRIPTION

GENERAL

TR8828C Series digitizers are optimized for digitizing and recording high frequency signals. The system modularity allows multiple channels, memory expansion, and mixing with other accessory modules or slower speed digitizers, thus providing flexibility for use in large and small system applications.

The signal to be digitized may be connected directly to the 0.510 V full-scale input or via a modular amplifier (LeCroy 6102 or 6103) if gain control is required. The TR8828C also has a high level 5.1 V input which is internally summed with the normal input. In addition to accepting large amplitude inputs, this allows algebraic addition of a timing marker, second analog signal or baseline correction.

Once armed by programmed command, the unit digitizes the input signal with 8-bit resolution and loads its associated memory. While the memory is being loaded, a DAC output reconstructs the data for user monitoring. This feature is useful in system testing and setup, and also may be connected to the trigger input to provide internally triggered operation.

The amount of memory is variable as determined by the number of memory plug-ins. Two MM8103A or MM8105 memories provide storage for 64K or 256K samples respectively; up to 14 additional plug-ins can be added as required, providing up to 512K or 2M samples respectively. The MM8104 memory is a special high speed version of the MM8103A and is used when larger memory size is not required or to conserve mainframe power or capacity. Only one is required. The MM8104 can be used with MM8103A units by changing a side-panel jumper and allows economical system expansion. Throughout the rest of this manual, the MM8104 will be referenced only when there is a difference in operation between it and the MM8103A/MM8105. Up to 100% pre and post-trigger recording is available on all units.

The TR8828C also has a burst mode in which samples can be loaded into the memory only when the stop trigger signal is greater than the threshold level. This mode may be used to divide the memory into segments for multiburst recording. The user must provide externally generated segment markers to allow data reconstruction.

The programmable parameters (memory size, pretrigger sample size, clock speed, and input offset) can be set or read at any time the unit is not digitizing. Remote control is available using the programmable arm (start digitizing) or stop trigger commands and the Look-At-Me flag (indicating data ready).

All modules plug into a mainframe which follows the CAMAC instrumentation and interface standards (see IEEE Standard

583–1975). A minimum system consists of one triple–width TR8828C Series and two single–width MM8103A/MM8105 (or one single–width MM8104) modules. Two cables, a 34–conductor and 50–conductor, connect the three modules electrically. This system can be controlled by any computer that has access to the CAMAC instrument mainframe through a controller module (e.g., LeCroy 8901A, 6010, etc.).

SPECIFICATIONS

Signal Input

Amplitude Range: 510 mV peak–to–peak.
Impedance: 50 Ω +3% DC; <7% reflection from 3 nsec edge; VSWR of <1.15 at 100 MHz.
Bandwidth: DC to >100 MHz (–3 dB), to >50 MHz (–1 dB).
Offset: Programmable over ±1/2 full scale in 256 steps.
Temperature Stability: ±1/2 mV/°C maximum.
Overload Recovery: ±1% in 25 nsec from a 1.5× overdrive pulse of <1 μsec duration.
Overload Protection: ±2.5 VDC; ±500 V for 30 nsec or ±100 V for 100 nsec with 50 Ω source.

High Level (X10) Signal Input

All characteristics same as above except
Amplitude Range: 5.1 V peak–to–peak.
Overload Protection: ±7.5 V DC.
Configuration: Internally summed with normal input.

Stop Trigger Characteristics

Slope: + or – set at side panel.
Level: ±2 V, adjusted and monitored from front panel.
Impedance: 50 Ω source.
Modes: In Normal Mode, trigger switches from pretrigger to post–trigger sampling; digitizing stops when post–trigger sampling complete. In Burst Mode (TR8828C only) clock is disabled whenever the trigger level is below the preset value.

Memory

Model	Storage/Unit	Speed
MM8103A	32K	100 MB/sec
MM8104	32K	200 MB/sec
MM8105	128K	100 MB/sec

Active Memory Size: Programmable in 16K sample increments up to the total size of memory installed (2M samples maximum if using MM8105 memory modules).
Pretrigger: Memory can be divided into pre and post–trigger sample storage, programmable from 0/8 through 8/8 in increments of eighths of active memory.
Burst Mode: Side–panel jumper option enables front–panel Stop Trigger Input to double as a clock control. (Pretrigger and programmed stop features can not be used).
Battery Backup: Data in memory is preserved when external power is removed.

Timebase

Internal: 200 MHz 0.01% crystal oscillator and divider provide sampling periods of 5, 10, 20, 40, 80, 160, or 320 nsec.
External: User clock can be supplied via 50 Ω front–panel connector; requires fixed 200 MHz ECL level only.
Clock Out: ECL level pulses available via front–panel connector.

Analog to Digital Characteristics

Resolution: 8–bit binary word (2 mV/LSB.)
DC Accuracy: Errors are less than ±1.5 LSB's plus 1/2 LSB quantizing error from best linear fit over entire range.
AC Accuracy: A reconstructed digitized pure sine wave has a minimum dynamic accuracy as follows:

Signal Frequency	Signal Amplitude	Effective Bits	Sig/Noise Ratio(dB)
To 5 MHz	80%	6.5	40
20 MHz	80%	6.0	37
50 MHz	50%	6.0	33
100 MHz	50%	5.5	26

Aperture Uncertainty: ±5 psec maximum.
Noise: RMS noise <1.7 counts, not including misconversions. The probability of a misconversion (defined as >3 counts) is typically less than one per million averaged over the entire amplitude range.

General

Connectors: All front–panel connectors are BNC, except FAST DAC, ARM BUSY, TRIG BUSY, and CDS (manual control enable) which are Lemo. Cables with either BNC or Lemo connectors are available from LeCroy.
Status Lights: Front–panel LED's indicate power and digitizing status.
Module ID: 8–bit side panel switch allows a unique user assigned module identification number which can be read to the dataway.

Power Requirements:

	+6 V	−6	24 V	−24 V
TR8828C	0.9 A	10.0 A	220 mA	175 mA
MM8103A	2.5 A	1.3 A	–	–
MM8104	2.5 A	1.3 A	–	–
MM8105	2.7 A	1.3 A	–	–

Internal Battery: Replaceable Lithium battery (lifetime >2 years) in each memory module and digitizer automatically becomes power source for memory and control registers.

Environment: Proper operation requires +15°C to +25°C intake air with sufficient flow to maintain temperature rise of exhaust air to <15°C (+30°C intake air allowed if sufficient airflow to maintain temperature rise of exhaust air to <10°C), humidity up to 90% non-condensing, altitude <10,000 ft above sea level. Storage temperature range is −10°C to +50°C.

Packaging: RF shielded module in conformance with the CAMAC (IEEE 583) Standard.

	Size	Height	Width	Depth
TR8828C	#3	221 mm	51 mm	292 mm
Memories	#1	221 mm	17 mm	292 mm

COMMANDS

Programming commands are listed in this section, while examples of the control sequence and a sample FORTRAN control program are contained in Chapter 4, Operating Instructions.

All CAMAC Dataway commands listed below except F(25) are disabled during conversion. To prevent possible noise induced by asynchronous digital switching, it is recommended that no unnecessary CAMAC commands be generated on the Dataway during the actual analog-to-digital conversion cycles (i.e., between arming units and receiving a Look-At-Me (LAM). The Z (Initialize) command from the CAMAC Dataway will clear and disable all LAM's and disable (unarm) the A-D converter, but will not otherwise affect control registers or stored data. All CAMAC function codes respond to A(0) only. An X- and Q-response is returned for all valid commands, except a Q-response requires that a valid data transfer has occurred (on a read or write command) or that the appropriate LAM is present (on a F(8) or F(27) command).

Parameter Setup, Status And Control Commands

Input Offset: F(1) reads from R9-R16; F(19) writes to W1-W8. Data is 8-bit binary representation of the input offset voltage where offset = 255 − N mV for N = 0 to 255.

Control Register: F(0) reads from R1–R16; F(16) writes to W1–W16. Data is 16–bit binary word, bit coded as follows:

Memory Samples (X 1024)		Sampling Period (nsec)		Pretrigger Samples (fraction of active memory	
0	16	0	5	0	0/8
1	32	1	10	1	1/8
2	48	2	20	2	2/8
3	64	3	40	3	3/8
4	80	4	80	4	4/8
5	96	5	160	5	5/8
.	.	6	320	6	6/8
.	.	7	EXT	7	7/8
.	.				
127	2048			8	8/8

W/R8 is not used; W/R16 is available to the user for storing programmable identification flag bit or event related information. Writing or reading it does not affect any other module parameter.

Trigger Arm: F(9) will arm the unit, and if the internal clock is used, starts digitizing, allowing the next trigger to initiate digitizing stop cycle. If the external clock is selected, F(9) will enable the clock input, but then requires an external clock to digitize and respond to a Trigger of F(25). All other commands are disabled when in the armed state.

Internal Trigger: F(25) generates an internal trigger (OR'd with external trigger input). Used in auto trigger modes or when calibrating, testing or demonstrating and no external trigger is available.

Module ID Word: F(3) reads an 8–bit binary value set on R1–R8 from switch located on bottom of module.

Memory Access Commands

Enable Read Mode: F(17) sets address counter to beginning of data record. Must be followed by F(2) or Z.

Read Data: F(2) reads two 8–bit samples on R1–R16 from the current memory location, then increments memory address by one. The two 8–bit samples contained in each 16–bit word are in binary representation, lower byte first. The first byte is the time vernier, see below. The next 15 bytes and the last 16 bytes may be inaccurate and therefore should be discarded. Read must be preceded by F(17) command (Enable Read Mode) to set address counter to beginning of data record. Q=1 while memory data is valid, going to 0 after last data word.

Trigger Time Vernier: The high-speed nature of the digitizer requires that four samples be simultaneously transferred to memory. R1 and R2 of first byte specifies which of the four bytes (of the next two words) starts the data record as follows:

R1–R2	First Sample
0	R1–R8 of 1st word
1	R9–R16 of 1st word
2	R1–R8 of 2nd word
3	R9–R16 of 2nd word

Note that even though this defines the location of the first sample, the actual data may be inaccurate until the 17th sample (9th word) is read.

LAM Commands

The LAM line on the CAMAC dataway indicates that a stop trigger has occurred and all post-trigger samples have been stored in memory.
Test LAM Status: The status of LAM also can be checked by F(8) or F(27) where a Q=1 response indicates that LAM is present. F(8) requires that LAM Enable be set.
Enable LAM: F(26) will allow a LAM to drive CAMAC dataway LAM line.
Disable LAM: F(24) will not allow a LAM to drive CAMAC dataway LAM Line. Z or C will disable both LAM's.
Clear LAM: F(10) will clear LAM.

CONTROLS AND CONNECTORS

Front Panel

Pwr/N (TR8828C Series): This dual LED flashes green when CAMAC N is asserted. Red indicates all power supply voltages are present on the control board of the module.
L/Rdy (TR8828C Series): This dual LED flashes green when the sampling clock has been enabled ready and the unit is digitizing and storing data. When red, it indicates that the digitizing sequence is completed and that internal LAM is set.
Pwr (Memory Module): This dual LED flashes green when the memory is being accessed. When red, it indicates that power is present.
Input: The analog input accepts 510 mV p–p signals with a DC offset in the range of ±1/2 full scale.
High Level Input: This input is similar to the Input described above except the input range is 5.1 V p–p. All other parameters remain the same.

Clock–In: This input is an ECL input terminated in 51 Ω. Data conversion is initiated by the positive edge, accepting an

input frequency of 200 MHz ±1 MHz with a 50% duty cycle. The input is protected against 5 A transients for 1 msec. The clock must last 16 cycles after the last data sample so that the transfer to memory of the last 8 data bytes is completed. At the users option the 51 Ω resistor can be terminated to ground or –2 V. The unit is shipped with the ground connection.

Clock–Out: This output provides an ECL compatible output of the 200 MHz clock. At the users option the ECL output may be pulled down to –5 V with a 110 Ω resistor. If no pulldown is selected, the output must be terminated externally with 50 Ω to –2 V. If the internal pulldown is selected, the output will drive 50 Ω to ground.

Stop: This input stops the sampling after the selected number of post–trigger samples has been stored. The minimum pulse duration is 8 nsec. The input is protected against 5 A transients for 1 msec. The threshold can be set and monitored from the front panel. The threshold range is ±2 V. Side–panel adjustments allow ± slope triggering and 51 Ω termination to ground or –2 V.

CDS: A low–level input forces the equivalent of a CAMAC N, which can be used to identify the digitizing module to the instrument controller. This input accepts TTL level signals and is pulled up to +5 V with 1 kΩ.

Fast DAC: This output provides the reconstructed input signal. This output is generated from data samples before they are stored in memory. This data appears at the selected sampling rate. The full scale range is approximately 1 V. The Fast DAC output requires a 50 Ω termination to ground.

Arm Busy: This output is TTL open collector output indicating the unit is sampling and is ready for a Stop Trigger. A side–panel jumper allows selection of the polarity of this signal.

Trig Busy: This output is a TTL open collector output indicating that the TR8828C Series has accepted an internal or external trigger and is acquiring the post–trigger samples. A side–panel jumper allows selection of the polarity.

Address: This 34–pin connector contains the address signals and control lines for writing to or reading from the memories. The signals are single–ended ECL except for the clock, which is differential. The address lines must be terminated by a memory module. The bus is unidirectional with the drivers in the TR8828C Series only.

Data: This 50–pin connector contains the databus from the TR8828C Series to the memory modules. The databus is 4 bytes wide, ECL, and must be terminated by a memory module. This bus is unidirectional with the drivers in the TR8828C Series only. The SPF line, indicating power–fail in the memory mod-

ules, is on this connector.

Stop Thr: Multiturn potentiometer adjusts threshold level of Stop Trigger of ±2 V range. Test point provides a voltage which corresponds to the level setting.

3 INSTALLATION

MECHANICAL SETUP OF JUMPERS AND SWITCHES

The TR8828C Series provides flexible configuration of its triggering and clocking. The Stop Trigger has four parameters selectable by means of side-panel jumpers: trigger slope, trigger busy and trigger arm polarity, and Burst Clock Enable. The trigger level is adjustable via the front-panel potentiometer. These should be set as desired. Figure 3.1 shows the side panel of the TR8828C and jumper selections.

The memory modules require some preparation before installation. First, the resistors which terminate the two cables must be removed from all but the last memory module on each cable. Removing all of the SIP resistor packs and the single 56 Ω resistor located in the sockets just behind the front panel accomplishes this. See Figure 3.2.

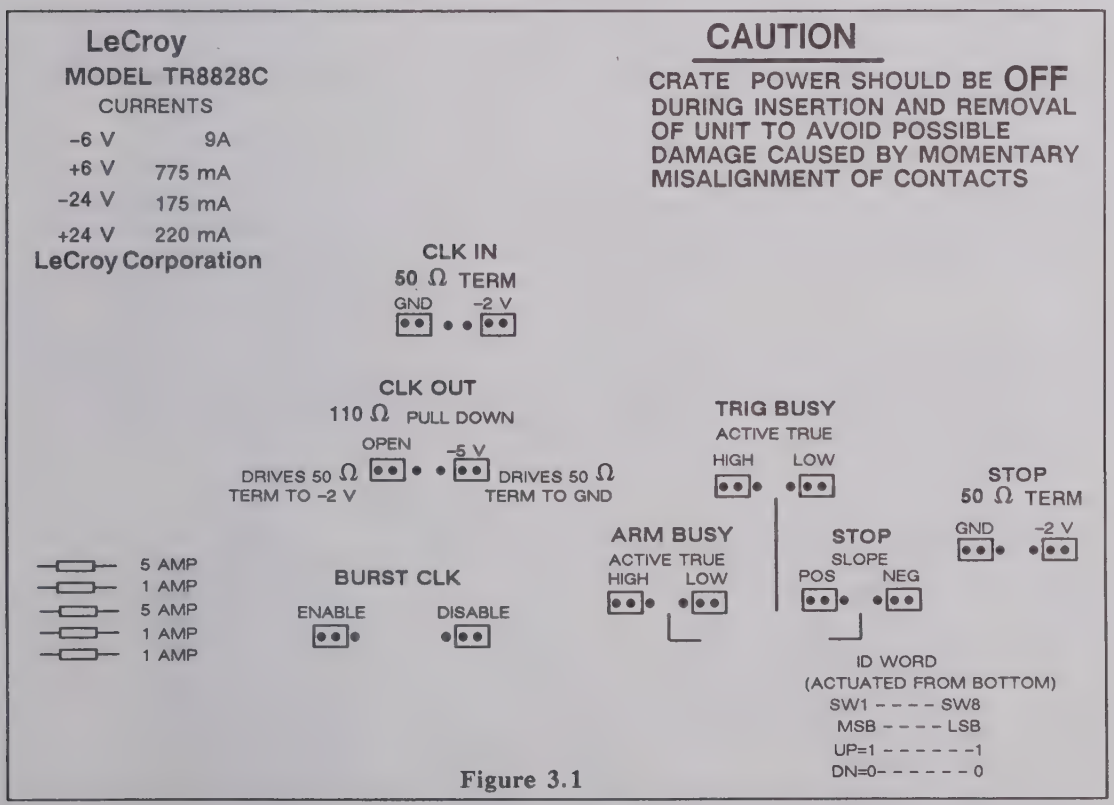


Figure 3.1

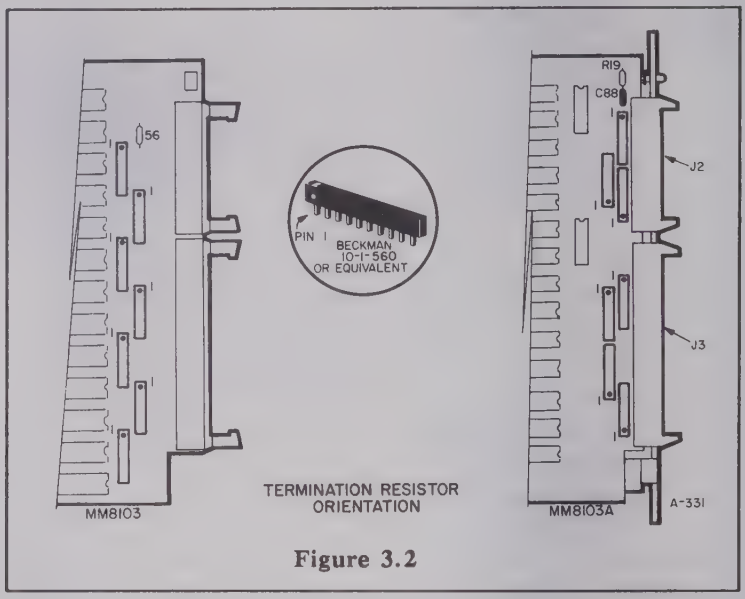


Figure 3.2

Now the front–panel switches must be set. These switches set the select codes in the binary fashion. Switch 1 sets the LSB and Switch 5 sets the MSB. Close all the switches on the MM8103A's. This sets the select code to 0. (A closed switch sets the bit to 0, an open switch sets the bit to 1). Set the first pair of MM8103A's to have a select code of 0, the next 1, the next 2, and so on until all of the MM8103A's have been given sequential select codes. Then set Switch 6 on one module of each pair to be open and the other Switch 6 of each pair to be closed.

Switch Positions

S5	S4	S3	S2	S1	Select Code
●	●	●	●	●	0
●	●	●	●	o	1
●	●	●	o	●	2
●	●	●	o	o	3
●	●	o	●	●	4
●	●	o	●	o	5

● = Closed o = Open

Memory MM8104

For a single MM8104, be sure the side–panel plug option is in the proper (8104) position for single–module (high speed) operation. Then set front–panel switches S1 thru S6 to 0. If multiple MM8104's and MM8103A's are used, the side–panel jumper should be put in the low speed (8103) mode and front–panel switches should be set as above.

Memory MM8105

For MM8105, Switch 1 sets the LSB and Switch 3 sets the MSB. Switch 4 on one module of each pair must be open and the other Switch 4 of each pair must be closed. Switches act in the same manner as for MM8103A.

Asserting F(3) and A(0) causes the 8–bit identification word to be read via R1–R8 of the CAMAC dataway. A switch array accessible from the bottom edge of the module allows convenient changing of the ID word. The ID word is factory set to 2, which provides LeCroy 6010 high speed averaging compatibility.

The TR8828C Series permits the user to select the termination for the ECL level External Clock Input. This is factory set to ground termination, but may be set to –2 V termination by means of side–panel jumpers.

The Clock Output provides an ECL level (–.8 V to –1.6 V) signal with internal 110 Ω pulldown to –5 V selectable by means of a side–panel jumper. If the internal pulldown is selected, the output will drive a grounded 50 Ω; with the internal pulldown disabled, an external pulldown to –2 V is required.

CABLING

The TR8828C Series requires two cables to connect the address and data buses to the memory module's recorder. The 34–conductor upper cable connects the address bus while the shielded 50–conductor lower cable connects the data bus. These cables are kept as short as possible to minimize crosstalk and reflections.

The cables are constructed with the following parts which are available through LeCroy or directly from the manufacturers as listed:

Connector 34 pin	LeCroy	#403–220–034
	3M	#3414–6034
Flat Cable 34 conductor	LeCroy	#592–030–034
	3M	#Scotchflex 3365/34
Connector 50 pin	LeCroy	#403–211–050 or
	3M	#3425–6050
Flat Cable 50 conductor	LeCroy	#592–040–050 or
	3M	# Scotchflex 3476/50

The input signal should be connected to either the normal input (510 mV p–p) or high level (5.1 V p–p) Input, and a trigger

source connected to the Stop Trigger input. If it is desired to trigger on the input signal, the Fast DAC output shall be connected to the Stop Trigger Input.

Since the TR8828C has a fixed input range, signal conditioning can be provided for with the Model 6103 dual–channel amplifier and trigger generator. Each amp channel can accept low or high impedance signals over a range of 50 mV to 50 V and provide an output to drive the TR8828C. The trigger generator allows programmable slope and level control from internal and external sources. When operating the 6103 with the TR8828C, the signal offset should be provided by the amplifier and the digitizer offset set equal to zero. Figure 3.3 shows typical cabling for 2–channel operation with external trigger conditioning.

Setup of the 6103 programmable amplifier is provided by a separate setup menu when using CATALYST software.

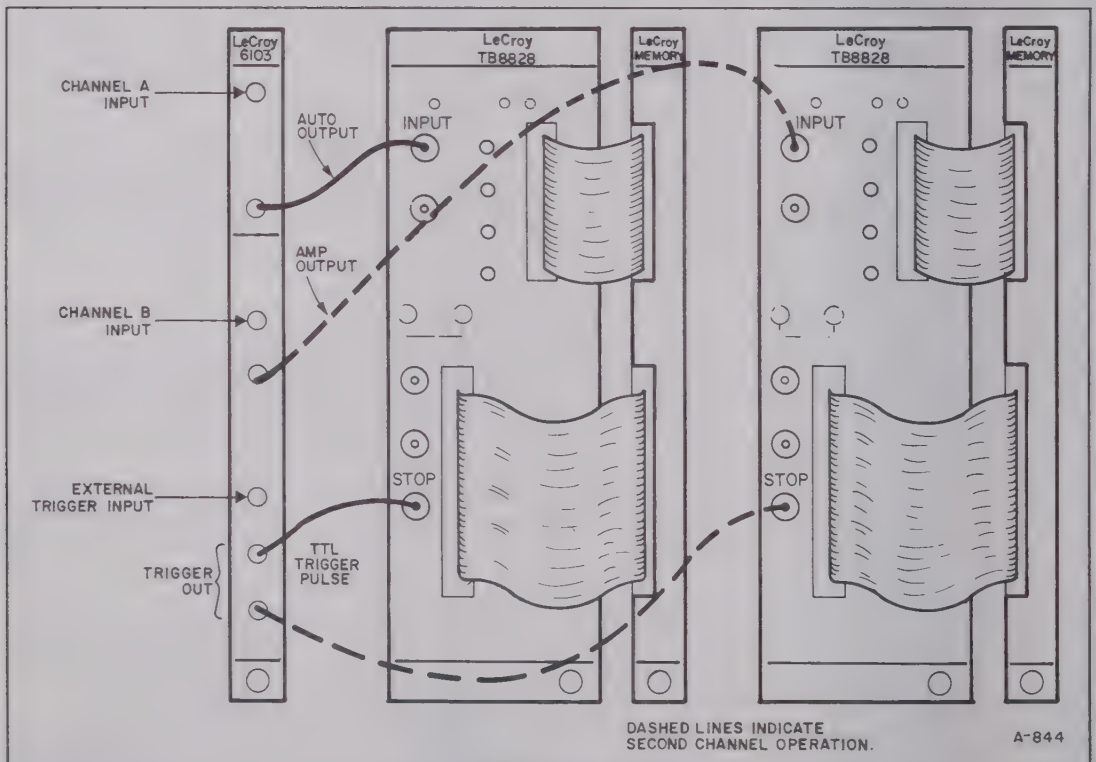


Figure 3.3

INSTALLATION IN MAINFRAME

The waveform recorder system is compatible with any CAMAC mainframe which provides adequate power. (See Specifications for the power consumption of each instrument).

With the power off, insert the waveform recorder in any station except the Control Station (the two rightmost locations in the mainframe), leaving room to the right for its associated memory module(s). Often it is best to avoid using the leftmost location, as cooling may not be adequate in this location. The location of the system (CAMAC N) is defined by the number printed on the mainframe for the slot identified by an arrow on the panel of the TR8828C Series. The last memory module must have a memory bus terminator. Cable the memory(s) to the digitizer to complete installation.

Ensure that the mainframe has sufficient clearance at the top to permit adequate airflow. During operation in the 8013A benchtop instrument mainframe, air-blocking baffles (Models BFP-1 and BFP-2) should be used to ensure proper cooling. Do not obstruct ventilation by placing papers or other objects on the top of the mainframe.

4 OPERATING INSTRUCTIONS

INTRODUCTION

The TR8828C Series waveform recorder is completely programmable. Three modes of program control are discussed:

1. Control of the TR8828C Series is demonstrated with a sequence of commands. While not specific to any controller, this serves as a step–by–step operation guide..

2. User written programs for control of the TR8828C Series with the GPIB standard (8901A or 6010) or by RS–232–C serial interface (6010 only) and the user's computer.

3. WAVEFORM CATALYST (Model (6900) provides digital storage oscilloscope operation of the system using keystroke commands of an IBM–PC, XT, AT or compatible personal computer and the GPIB (IEEE–488) bus. CATALYST software requires either the 8901A or 6010 to be the control module in the instrument mainframe.

All three use CAMAC Function (F), subaddress (A), and mainframe slot (N) to program operation. When programming GPIB operation, the LeCroy 8901A is programmed in decimal codes, while the 6010 provides an ASCII command structure with multiple options and high speed signal averaging. In WAVEFORM–CATALYST software control the user initiates action with keystroke commands and eliminates programming.

PROGRAMMED OPERATION OF THE TR8828C

This section provides a sequenced guide to programming the TR8828C and interpreting the decimal control words. For background reading, refer to Section 6 of this manual or to LeCroy AN–33 *Introduction to CAMAC*.

Power Up

After applying power to the waveform recorder and memories, a Z (reset) command should be issued.

Setting Control Word

Because the control register has battery back–up, it will always contain the last control word written to it. When the waveform recorder is not in the armed state, the control word may be read and changed using the F(0) and F(16) CAMAC functions.

The control register is 16 bits in length and programmable via the CAMAC dataway using F(16) and A(0) with W1 through W16. Asserting F(0) and A(0) on the CAMAC dataway will enable the control register onto R1 through R16. The control register contains the user bits, memory size, sampling period, and pretrigger size in the following format:

W16 . . . W1
R16 . . . R1
U0 M6 M5 M4 M3 M2 M1 M0 X S2 S1 S0 P3 P2 P1 P0

Where U0 is a user bit
M0, . . . M6 is the memory size
X not used, state does not matter
S0, S1, S2 is the sampling period
P0, P1, P2, P3 is the pretrigger size

The control register is decoded as follows:

Binary							Decimal	Value
M6	M5	M4	M3	M2	M1	M0		
0	0	0	0	0	0	0	0	16K bytes
0	0	0	0	0	0	1	1	32K bytes
0	0	0	0	0	1	0	2	48K bytes
0	0	0	0	0	1	1	3	64K bytes
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127	2048K bytes

S2	S1	S0		
0	0	0	0	5 nsec
0	0	1	1	10 nsec
0	1	0	2	20 nsec
0	1	1	3	40 nsec
1	0	0	4	80 nsec
1	0	1	5	160 nsec
1	1	0	6	320 nsec
1	1	1	7	external clock

P3	P2	P1	P0		
0	0	0	0	0	0/8 of memory
0	0	0	1	1	1/8 of memory
0	0	1	0	2	2/8 of memory
0	0	1	1	3	3/8 of memory
0	1	0	0	4	4/8 of memory
0	1	0	1	5	5/8 of memory
0	1	1	0	6	6/8 of memory
0	1	1	1	7	7/8 of memory
1	0	0	0	0	8/8 of memory

PROGRAMMED OPERATION (continued)

P0–P3 set the pretrigger size, the fraction of the selected memory size that will precede the stop command. For example, if a memory size of 32K and a pretrigger size of 3/8 are selected, then after a digitizing cycle, the first 12K bytes of memory will contain data sampled just prior to the stop command and the last 20K bytes the data sampled just after the stop command.

S0–S2 set the period of the sampling clock. As shown above, you may choose any of seven internal periods or an external period of 5 nsec. The external clock should have a 50% duty cycle.

M0–M6 set the size of the data record. These bits select any memory size from 16K to 2M in 16K increments.

The user bit U0 can be set and read and is maintained during power down. This bit has no internal function so it can be used for storing status, run number, etc., by the user.

The definition of the control word using decimal notation for the control bits is:

CW=PD + (SD X 16) + (MD X 256) + (UD X 32,768)

Setting Offset

The offset register is also battery backed–up and will contain the last value of offset written to it. Analog signals at the input to the TR8828C Series may be offset by 255 mV with the offset register. The offset register is 8 bits in length and is programmed via the CAMAC dataway. Asserting F(19) and A(0) will write W1 through W8 to the offset register. Asserting F(1) and A(0) will read back the offset register in R9 through R16.

Writing 0 to the offset register allows input signals between ground and –510 mV to be digitized. An offset of 127 allows signals between –255 mV and +255 mV to be digitized. An offset of 255 allows signals between ground and +510 mV to be digitized. Intermediate value of offset will displace the input signal correspondingly.

Offset Value	Range of Input	Use
0	–510 mV to 0 mV	negative signal
127	–255 mV to +255 mV	bipolar signals
255	0 mV to +510 mV	positive signals

Assistance in determining the optimum offset level can be had by observing the digitized signal at the FAST DAC output. The offset is calibrated so that the actual offset will differ from the programmed request by less than ±2% of the full scale (±5.0 counts). If 2% accuracy is not sufficient, the user can always obtain the exact number of offset counts desired by writing an offset, reading back the actual offset and then adjusting the requested offset to obtain the desired final offset.

For applications in which highest precision is needed, the user should be aware that the DC level of the input can have some effect on accuracy. If the input is biased to the exact center of full scale then it will toggle between outputs of 10000000 and 01111111. This situation (with all bits toggling) will generate enough noise to occasionally cause other readings. In all cases the RMS variation of the output will be less than two counts; typically the RMS variation is less than one count. In order to avoid the possible inaccuracy introduced by this effect it is recommended that the user not apply a DC level to the input (or request an offset) corresponding to 127 counts. Similar but smaller effects may be observed at other DC input levels which correspond to the toggling of many bits (e.g. 63 counts).

Applications using the 6103 programmable amplifier should set offset at the amplifier and keep digitizer offset equal to zero.

Sampling the Waveform

Once the pretrigger, sampling period, memory size, and offset are as desired, input waveforms can be recorded. The F(9) command starts the sampling and the memory begins storing data in a circular fashion. While digitizing, the TR8828C Series is considered to be in the ready state. Only the stop command [F(25) and A(0)], the STOP input, or the initialize signal Z can remove the TR8828C Series from the ready state. Only one CAMAC function code command will be recognized, i.e., F(25) and A(0). All others will be ignored and will generate Q=0.

The waveform recorder fills the memory sequentially. Upon reaching the end of memory (length set by the control word) the recorder starts at the beginning and writes over old data. Sampling will continue until a stop trigger is received. There are two ways to stop the waveform recorder: the CAMAC function F(25) or the Stop Trigger Input. The trigger level is adjustable ±2 V via the front-panel potentiometer and may be monitored via the test point. When operating in the external clock mode, a stop trigger will not be recognized unless an external clock is being supplied. Until this occurs, the unit will disable all CAMAC commands.

Following receipt of the trigger, the waveform recorder continues operation until the selected number of post-trigger samples have

PROGRAMMED OPERATION (continued)

been digitized and stored. The internal LAM is then set. If enabled via F(26) and A(0), LAM will be asserted on the dataway. LAM can be cleared via F(10) and A(0) or Z. Asserting F(9) and A(0) and starting a new digitizing cycle will also clear the LAM. To determine if the sampling has finished, the LAM or LAM status can be tested with F(8) or F(27) respectively. An alternative to polling the LAM is to enable the LAM with F(26) before starting to sample and then using the crate LAM to interrupt the processor with a service request.

Data Readout

Digitized data can be read from the memory modules via commands sent to the TR8828C Series. Asserting F(17) and A(0) will load the starting address of the data in memory from an internal register into the address counter. The data can then be read by generating successive F(2) and A(0) commands. Q will be true (Q=1) for every valid data sample. After the last sample is read, further F(2) and A(0) commands will produce Q=0. The data can be read again by asserting F(17) and A(0) to reload the starting address and then using F(2) and A(0) to read the data.

Data is read sequentially from the memory modules, 2 bytes at a time.

R1–R8 contain the first byte and R9–R16 contain the second. This maximizes the transfer rate to the computer. The first word (R1–R16) that is read with F(2) and A(0) after F(17) and A(0) is a status word. If this word is zero, then the first byte (R1 – R8) of the next word is the first byte of the data record. If the status word is a one, the second byte R9 – R16 of the next word is the first byte of the data record, etc. Because the data bytes are pipelined into the memory, the first and last 16 bytes of the data record will be garbled.

The reliability of data provided by the TR8828C is carefully checked by the factory. Prior to shipment all units undergo thorough testing, including operation during temperature cycling and at the maximum specified temperature. Some tests include the digitization of slow ramp signals and many frequencies of sine waves. The output is then compared with the known input. On very rare occasions a signal data word will have a bit error. A particular bit which should be on may be off or vice–versa. This type of error may be found in all systems which use flash ADC's near their maximum conversion rate. All units are factory checked for a conversion error rate. Typically it is less

than one wrong data sample per million data words using a 1-million sample test.

SAMPLE FORTRAN PROGRAM

The following FORTRAN program illustrates the use of the TR8828C Series and Memory Modules. The program uses a subroutine called CAMO every time a command is transferred to the instrument mainframe and digitizer:

```
C example program for the TR8828C Series
      PROGRAM SAMPLE
C the subroutine  CAMO executes one CAMAC cycle
C the parameters for the subroutine
C  CAMO  (SLOT,F,A,W) are
C          SLOT    for which N is asserted
C          F       value of function code to be asserted
C          A       address to be asserted
C          W       data written to W1-W16

C the subroutine CAMI executes one CAMAC cycle
C the parameters for the subroutine CAMI(SLOT,F,A,X,Q,R)
C are
C          SLOT    for which N is asserted
C          F       value of function code to be asserted
C          A       address to be asserted
C          X       value of X returned (true or false)
C          Q       value of Q returned (true or false)
C          R       data read from R1-R16

C the subroutine CRATE sets crate address to the value of the
C argument
C the subroutine PULSEZ generates a common Z to the
C addressed crate

      INTEGER SLOT,MEM,PERIOD,PRETRG,USER
      INTEGER CONTRL,OFFSET
      INTEGER PNTR,TEMP,DATA(1024)
      LOGICAL X,Q

C address waveform recorder in slot 10 of crate 1
      CALL CRATE(1)
      SLOT=10

C pulse Z reset line to reset waveform recorder
      CALL PULSEZ
C set memory size to 16K (range 0-31)
      MEM=0

C set sampling period to 5nsec (range 0-7)
      PERIOD=0
C set pretrigger samples to 4/8 of memory size (range 0-8)
```

PROGRAMMED OPERATION (continued)

```
      PRETRG=4

C set user bits to 1
      USER=1

C write to control register using F(16) and A(0) to set memory
C size, sampling period, pretrigger samples, and user bits.
      CONTRL=USER*32768+MEM*256+PERIOD*16+PRETRG
      CALL CAMO(SLOT,16,0,CONTRL)

C set input offset to center 0 V input (range 0-255)
      OFFSET=128

C write to offset register with F(19) and A(0)
      CALL CAMO(SLOT,19,0,OFFSET)

C start sampling and reset LAM with F(9) and A(0)
      CALL CAMO(SLOT,9,0,0)

C issue stop command, F(25) and A(0), then check for LAM
C if LAM is not set meaning that the recorder is not finished,
C then issue another stop and check LAM again...


C the additional stops are required because the stop trigger is
C disabled during the first cycle through the memory to
C insure that the pretrigger samples are written

  100 CALL CAMO(SLOT,25,0,0)
      CALL CAMI(SLOT,27,0,X,Q,TEMP)
      IF(.NOT.Q) GOTO 100

C load starting address into memory address counter
C and initialize data read-out with F(17) and A(0)
      CALL CAMO(SLOT,17,0,0)

C read status word to get pointer to first valid data byte
C add 16 to pointer so that garbled bytes are skipped
      CALL CAMI(SLOT,2,0,X,Q,PNTR)
      PNTR=PNTR+16

C read waveform data (1024 bytes) using F(2) and A(0)
      DO 200 I=0,511
         CALL CAMI(SLOT,2,0,X,Q,TEMP)
C get data byte from R1-R8
         DATA(2*I+1)=TEMP.AND.255
C get data byte from R9-R16
  200    DATA(2*I+2)=(TEMP/256).AND.255
```

```
C the array DATA now contains 1024 8-bit samples
C with values of 0 to 255
C the PNTR points to the first valid sample

      STOP
      END
```

PROGRAMMING VIA 8901A AND 6010

The following is a condensed outline of commands to assist a first time user of LeCroy's TR8828C Series waveform recorders in combination with the LeCroy Model 8901A CAMAC to GPIB interface.

It is the most basic information required, just sufficient to operate the system, assuming the user is generally familiar with the GPIB controller (computer) being used. It is suggested that the individual manuals and technical data sheets on these modules as well as IEEE-583 CAMAC and 488 GPIB Standards be used if a more thorough understanding of the system is desired.

8901A Guide

For purposes of this example, assume that the Model 8901A is at GPIB address 1 and the Model TR8828C is in slot 3. The operations that will be performed are:

Initialize the instruments upon power on and initiate sampling
w*ait for trigger*
e*nable TR8828C for reading*
r*ead data out in high-speed mode*
r*ead acquisition parameters*

The implementation of this sequence (from the GPIB system controller) is given below. The following notation is used:

OUT x,y,...
: Indicates a transfer from the GPIB controller to the 8901A. It includes addressing the 8901A to Listen, sending the data byte(s) to it, and then sending the GPIB Unlisten command.

IN B1,...Bn,R
: Indicates a n+1 byte transfer from the 8901A to the GPIB controller. (B1 ... Bn) are data bytes, R is the CAMAC response byte with X and Q. It includes addressing the appropriate 8901A to Talk, reading the data byte(s) into the computer, and then sending the GPIB Untalk.

TALK
: Indicates sending out the GPIB Talk address to the specific 8901A. This is used to execute a CAMAC cycle when no data is to be returned. The IN command may be substituted if desired (e.g., to allow monitoring the CAMAC response bits X and Q)

The following shows segments of a control program using the LeCroy 8901A and the TR8828C Series. The above sequence from initialize through data readout is outlined.

Initialize the Instruments

OUT 33	Initialize the crate by sending CAMAC Z
TALK	Execute CAMAC cycle by addressing 8901A to Talk
OUT 98	Program 8901A to return 16 bits of data and the CAMAC response byte
OUT 16,0,3,D1,D2	Program instrument's parameters by sending F(16), A(0), N(3), D1, D2 (D1, D2 are the parameter bytes)
IN B1,B2,R	Execute CAMAC cycle and get CAMAC response
OUT 19,0,3,D1	Program offset in TR8828C to value D1
IN B1,B2,R	Execute CAMAC cycle and get response

Enable LAM

OUT 65	Program 8901A to set SRQ on LAM
OUT 26	Enable TR8828C to generate LAM by sending F(26) (note that since the A and N have not changed it is not necessary to resend them)

Initiate Sampling

OUT 9,0,3	Initiate sampling in the TR8828C with a F(9),A(0),N(3).

Wait for Trigger

At this point, the TR8828C is waiting for a trigger (either external or from an F(25) sent to it). After the trigger occurs and the module is finished acquiring data, it will generate a service request.

Perform a serial poll to determine which instrument set LAM (assuming there is more than one).

OUT 64	Disable the 8901A from generating another SRQ
SPE	Send the GPIB serial poll enable command
IN R,L1,L2,L3,L4	Read in the 5 status bytes (R is the CAMAC response byte and L1 – L4 are the current state of the LAM lines).
SPD	Send the GPIB serial poll disable command

Enable TR8828C for Reading

OUT 10,0,3	Clear LAM in TR8828C with F(10),A(0),N(3)
TALK	Execute CAMAC cycle by addressing 8901A to Talk
OUT 17,0,3	Enable read mode in the TR8828C with an F(17),A(0),N(3)

TALK	Execute CAMAC cycle by addressing 8901A to Talk

Read Data

OUT 2,0,3	Send F(2) to TR8828C – command to read data
IN B1,B2,R	Read two words to determine sample location
IN B1,B2,R	
OUT 106	Set 8901A up for a high speed block read of 16–bit data words
IN B1,...Bn,R,0	Execute a CAMAC cycle and read all of the data out (at end of data, module sets Q to 0. The 8901A then sends the response byte followed by a 0 with the GPIB EOI bit set)

Read Acquisition Parameters

OUT 98	Program the 8901A for a 16–bit data word
OUT 0,0,3	Tell the TR8828C to send its parameters F(0),A(0),N(3)
IN B1,B2,R	Execute CAMAC cycle and get 2 bytes containing its acquisition parameters and the CAMAC response byte
OUT 1,0,3	Read the TR8828C input offset
IN B1,B2,R	

6010 Guide

The 6010 control module provides the same functions for the the TR8828C Series. However, it uses ASCII control commands rather than decimal words. A TR8828C control subroutine using the 6010 is shown below.

```
# indicates comment

integer *2 crate                    GPIB Address of Crate
integer *4 LAM                      LAM Sta
# assume TR8828 in slot 3
# subroutines
# CCRATE (GPIB ADDR) - sets GPIB address for following
GREAD & GWRITE calls.
#GREAD (var, count) - reads bytes into variable from GPIB
#GWRITE (string) - writes command string to GPIB

Call CCRATE (ADDR); setup GPIB address for crate
Call GWRITE ('F 16; A 0; N 3; W32772; e')
Using F16 write control word to set memory size, sampling period,
and pretrigger to the TR8828 in slot 3
Call GWRITE ('F 19; W 128; e')
     set offset to zero;
Call GWRITE (MASK 1, 80; MASK 5, 3;)
```

```
Set service request mask, mask1 = send SRQ on operation complete; mask 3
= only look at LAM when operation done.
Call GWRITE ('F 26; e; F 9; e')
  Enable LAM on TR8828C and arm
ON SRQ
SPE      Serial Poll Enable
read STB      Read Status Byte
SPD      Serial Poll Enable
Call GWRITE ('CFMT OFF, WORD, BIN; CBLS 8192; CAMAC_WIDTH
2;')
-set block format off, 16-bit read, binary representation; blocksize of 8192;
tells 6010 to read 16-bit word from CAMAC
Call GWRITE (F 10; e; F 17; e; F 2; e, RB')
-clear LAM, set pointer to beginning of memory, read data
Call GREAD (NEW DATA, 8192)
-read 8192 samples into buffer called NEWDATA.
```

USING THE TR8828C WITH CATALYST SOFTWARE

WAVEFORM–CATALYST Software (LeCroy Model 6900) is an IBM–PC, XT, AT (or compatible) based digital storage oscilloscope software package for LeCroy modular recorders, including the TR8828C Series. The software interfaces to the 8901A or 6010 controller via GPIB and provides control, display, manipulation and archiving of digitized data. Single keystroke commands make the system easy to learn and to use. No prior knowledge of computers, programming or interface standards is required. Figure 4.1 shows the waveform display generated by CATALYST software and the TR8828C waveform recorder.

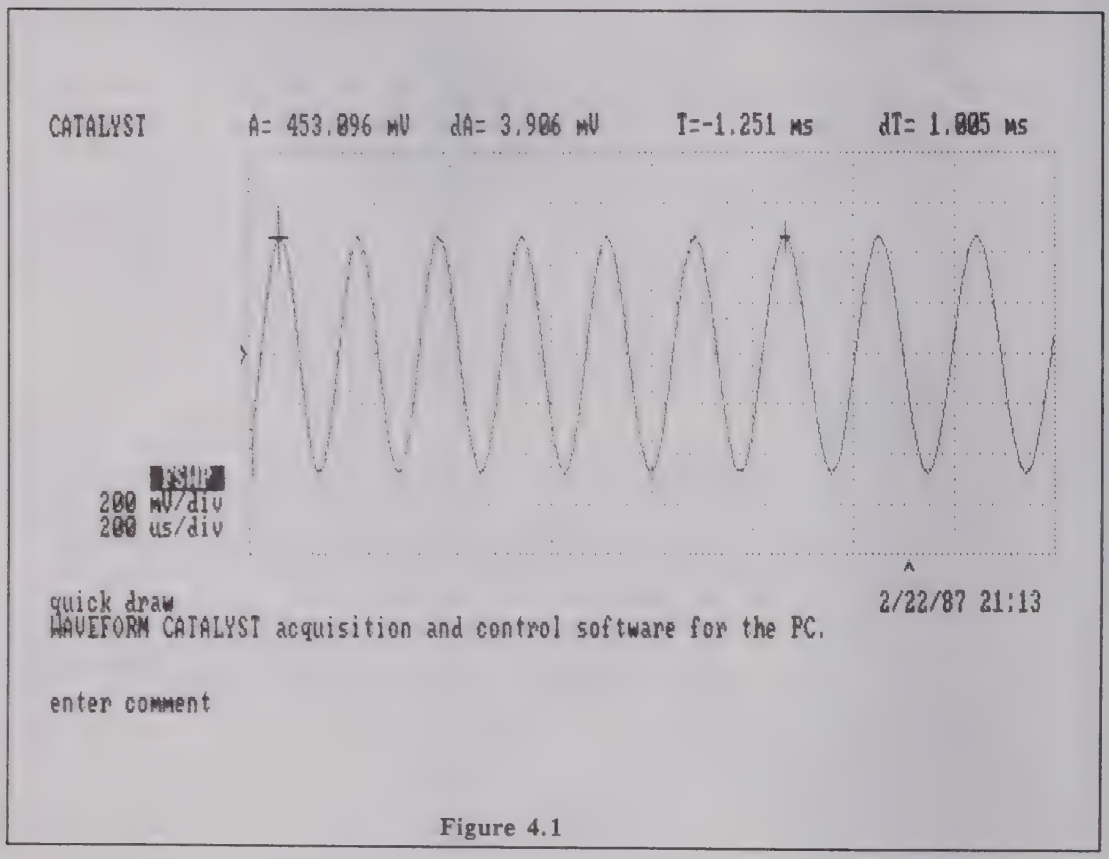


Figure 4.1

To run the TR8828C with CATALYST software, first refer to the WAVEFORM-CATALYST's User's Manual for a guide to configuring and assembling the personal computer.

The CATALYST Software can control multiple channels from the entire family of LeCroy modular digitizers. Each instrument mainframe (8013A or 1434A) can house multiple digitizing modules according to available space and power. Operation of the software is transparent to the use of the Model 8901A and the 6010 GPIB controllers. After configuring the digitizing hardware per Chapter 3 of this manual and following the software installation instructions, you should become familiarized with

software commands executed from the PC keyboard by referring to the CATALYST Quick Reference Card or by pressing **F1**.

The following example illustrates a sequence of CATALYST commands used to acquire and display data from a TR8828C placed in slot 6 of the instrument mainframe. The GPIB address on the 8901A or 6010 has been set to 12 on the front-panel dip switch.

Most of the primary commands in the system are single keystrokes; that is, only the key corresponding to the first letter of the command must be pressed in order to execute that function. For instance, if the modules in your system are configured properly, pressing **A** selects auto trigger mode which repeatedly arms and triggers the module. For some commands, however, additional information is required, in which case CATALYST prompts the user for the information needed. An example of this type of command is Write data. When W is pressed, the message "enter file name:" is displayed. For still other commands, a new list (or menu) of commands is displayed at the bottom of the screen. While a menu is displayed, any command in the list may be entered by pressing the key corresponding to its first letter. Pressing the space bar erases the command menu and returns the keys to their primary functions. G is an example of this command type since it activates the grid format menu.

The following example illustrates a sequence of CATALYST commands used to acquire and display date from a LeCroy TR8828C 200 megasample/sec digitizer which has been placed in slot 6 of the instrument mainframe. The GPIB device address on the mainframe is 12.

Install WAVEFORM-CATALYST to your floppy or hard disk using setup instructions in the CATALYST manual.

Turn instrument mainframe and computer on.

Load WAVEFORM-CATALYST by pressing Ctrl, Alt and Del keys simultaneously.

When CATALYST is loaded, choose digitizing parameters as follows:

COMMAND	RESULT
L(ist modules)	The list of modules in the system is printed along the bottom of the screen. Select the number of modules you want to operate.
3. 8828	Setup menu will appear. Use arrow keypad (left, right, up, down) to move reverse video on screen to digitizing parameter you wish to adjust.

Press Enter on menu and select desired parameters.

e.g.:

NAME	TR28
ACQUIRE	Yes
GPIB ADDR	12
SLOT	6

Choose sampling rate, memory length, pretrigger, etc. Press Help for explanation of TR8828C parameters.

You may store this setup using Write in the setup menu. Selecting the file name sd8828.cat causes the current menu values to be loaded automatically each time CATALYST is begun. Pressing the space bar exits the setup menu.

Select which trace to display:

COMMAND	RESULT
1 Trace Number	Traces are numbered from 1 to 4 from the bottom to the top of the screen. CATALYST prompts for name of channel to be displayed.
TR28	Enter four digits corresponding to name of module as defined in setup menu.
Grid	Select how many grid boxes you want (Single, Dual, or Quad). If you have multiple traces displayed, this function permits you to display them separately or overlayed.
	Connect input signal and trigger input (STOP on TR8828C)
	Select CATALYST triggering mode
Auto	Data will be displayed from TR8828C with parameters selected.
	Trace may be expanded, positioned and operated upon with cursors. Reverse video on channel name (at left of screen) indicates which trace CATALYST keys are operating on.
	Note that if you have more then one channel operating, each memory must be read out before any recorder can be rearmed. The active trace is selected by moving the primary cursor (selected by pressing the Home key) up and down.
	To turn off an undesired trace, press the trace number you wish to remove. When prompted for trace name, press return without entering any ID.
	The screen should now be updating with data from the TR8828C. Select other triggering modes (Normal, Single, Manu-

al) by pressing N, S, or M, respectively. Other CATALYST functions are highlighted in the user's manual and CATALYST user's card.

Additional Help screens like the one pictured in Figure 4.2 are available for each module type in the List Module menu. To access these help files, enter the Setup Menu and press **Help**.

When used with the 6103 programmable amplifier, gain, offset and triggering can be controlled by the separate setup menu for the 6103.

```
                TR8828C - 200 MSample Transient Recorder

8 bit resolution
upto 2M memory (512k for all units before ECO# 2005)
512 mv peak to peak signal range

Notes:
  1. If an external clock is desired, the PERIOD must be set to EXT and
     a 200 MHz clock must be used
  2. Offset range is -256 mv (unipolar positive signal) to 256 mv (unipolar
     negative signal)
  3. Full scale volts is provided as a correction factor for amplitude incase
     an amplifier or attenuator is used.  Valid range is .1mv to 100 v
  4. The first and last 16 samples may have been overwritten and are therefore
     set to zero so that erroneous data will not be displayed.
  5. Pre-trigger sample size (PTS) ranges from 0 to 8 eighth's of memory
  6. Data is displayed blocks of 8k words.  Multiple blocks may be view
     simultaneously by assigning the module to more than one trace and paging
     to the desired blocks.
  7. Memory size is selectable in 16k steps upto 2 Megawords.  It is possible
     to read in and store less than 16k points but 16k points will be sampled.


                        press any key to continue
```

Figure 4.2

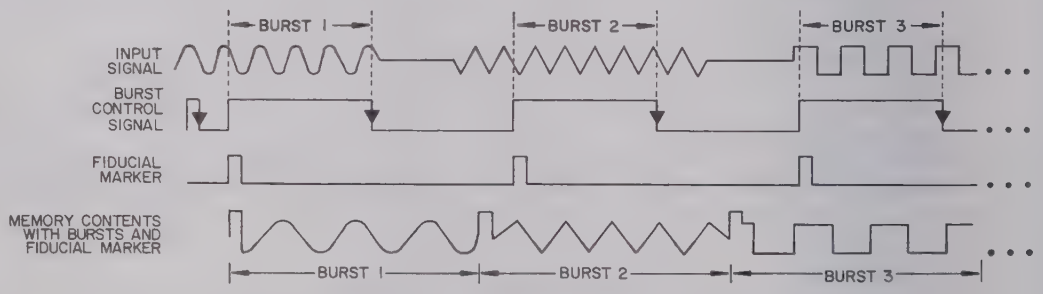
BURST MODE

In the normal mode of operation, the minimum memory size is 32K bytes and the maximum size is 2 megabytes. Active mem-

ory is a portion of physical memory defined by user in multiples of 16K bytes. Memory cannot be read out until all of the active memory has been addressed with data or intentionally padded with "non-data".

In the "normal mode", contiguous waveform samples collected at the selected sampling rate are loaded into consecutive memory addresses. Pretrigger sampling is available from 0/8 to 8/8 of active memory. The duration of the digitized waveform depends on sampling rate and total memory employed.

Burst mode is a feature of the TR8828C for units having ECO level greater than 1002 and is described in Figure 4.3 and Application Note 2014 (in the Service Package). It allows efficient use of memory when digitizing many short record segments back to back in the LeCroy memory module. Burst mode is selected by jumper on the side panel of the instrument. In this mode the front-panel Stop Trigger Input is used as a clock control such that data will not be transferred to memory as long as the trigger level is present. The user can select (via side-panel jumper) the slope which stops data into memory. When the clock is asynchronous to the burst stop signal, the length of the acquired burst may vary by a few samples. To ensure proper registration, it is recommended that a time reference pulse be injected into the High Level Input at the beginning of each segment in order to identify each segment when reconstructing the data from memory.



NOTES:

1. BURST MODE SELECTED BY SIDE PANEL JUMPER.
2. STOP SLOPE ABOVE IS SET TO NEGATIVE ON SIDE PANEL.
3. THRESHOLD ON TR8828C IS SET TO +50mV IN THIS EXAMPLE.
4. FIRST CONTROL PULSE REQUIRED TO EXECUTE ARMING OF RECORDER.
5. BURSTS ARE ACCEPTED UNTIL RECORDER MEMORY IS FILLED.

A-641

Figure 4.3

Pretrigger sampling must be set to 0/8 when using the burst mode.

To begin a burst mode acquisition, a short pulse above the threshold must be applied.

Note that the first 16 waveform samples belonging to the first burst are not valid data. Similarly, the last 16 samples belonging to the last burst must be discarded. However, all of the remaining waveform samples contained in all other bursts are valid.

BURST GENERATORS

Burst gate signals can be generated by LeCroy modular gate and delay generators Models 2323A and 4222. The 2323A provides manual or programmable dual channel variable gate functions with fixed delay widths and multiple options for TTL or NIM output levels and 50 nsec resolution.

Follow the instructions in the 2323A manual to set the output levels to TTL. To arm the TR8828C in Burst Mode, set Channel A gate to 50 nsec. Use the Channel B gate to set to the desired length of the Burst. The trigger applied to Channel B start input initiates the Burst. Set Channel B Delay to 50 nsec (DEL is set for TTL on the 2323A side panel) to provide a fiducial marker at the High Input of the TR8828C. The timing diagram in Figure 4.4 shows the sequence.

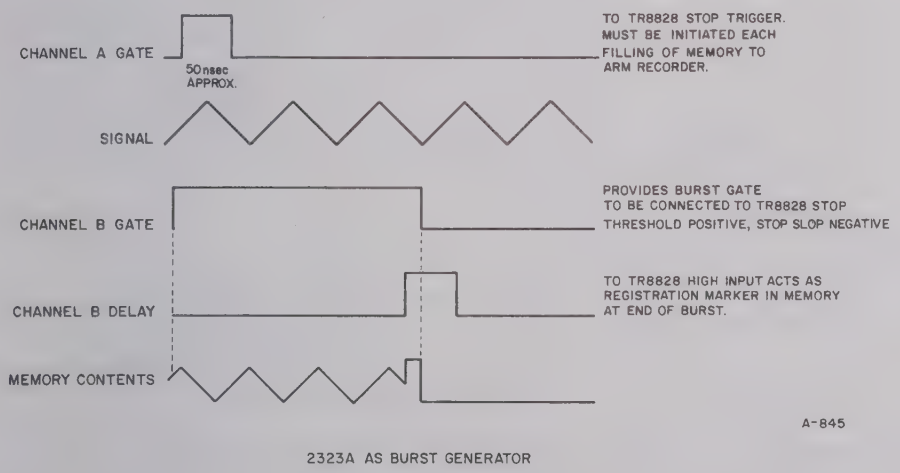


Figure 4.4

For delayed trigger burst operation (Figure 4.5), the system trigger is fed to START on Channel A, which initiates the trigger delay duration. Take the NIM out signal from Channel A into the start of Channel B. Set the gate of Channel B equal to the Burst recording on time. Note that depending on the polarity set for the output levels, the 2323 start threshold will require adjustment to ensure proper triggering of the unit.

MODEL 4222 BURST GENERATION

The 4222, operating in coupled mode, provides a programmable gate suitable for timing when data is stored in digitizer memory during TR8828C Burst Mode operation. Set the side panel of the 4222 to retrigger enable, GATE ON for channels 1, 2, 3, 4, and set the slope of the system start signal. Connect the system trigger to TRIG IN on the 4222. The unused TRIG IN connection should be terminated with 50 Ω. The programmable delays on channels 1 through 4 are set as follows:

Gate 1	Delay 1: Rising edge of GATE pulse 1
	Delay 2: Falling edge of GATE pulse 1
Gate 2	Delay 3: Rising edge of GATE pulse 2
	Delay 4: Falling edge of GATE pulse 2

The duration of each gate is delay 2 (4) minus delay 1 (3). Gates 1 and 2 are available from OUT 1 and 3 respectively. Apply the output from OUT 1 to the STOP TRIGGER input of the TR8828C. Refer to Figure 4.6 for a timing diagram and example. As shown in the figure OUT 3 can be used to provide a fiducial timing mark indicating where two burst of data adjoin in memory. The 1 nsec resolution of the 4222 and excellent jitter allows precise placement of the Burst Gate in reference to the system trigger. By synchronizing the system trigger to the TR8828C digitizing clock the burst gate width can be tuned to repeatedly provide the same number of samples in each burst.

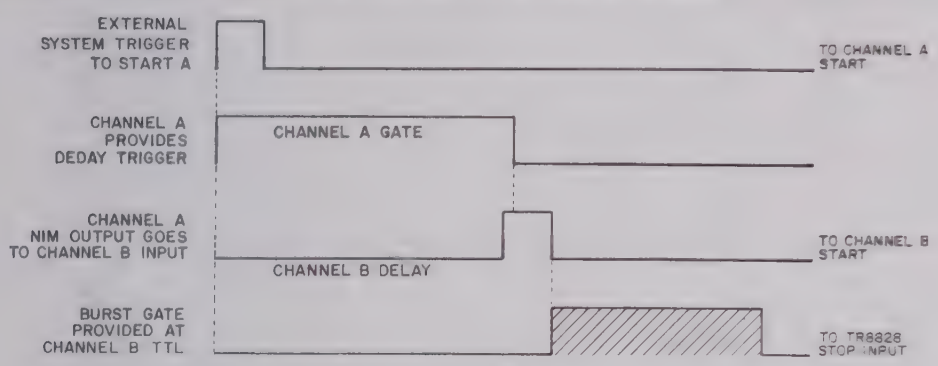


Figure 4.5

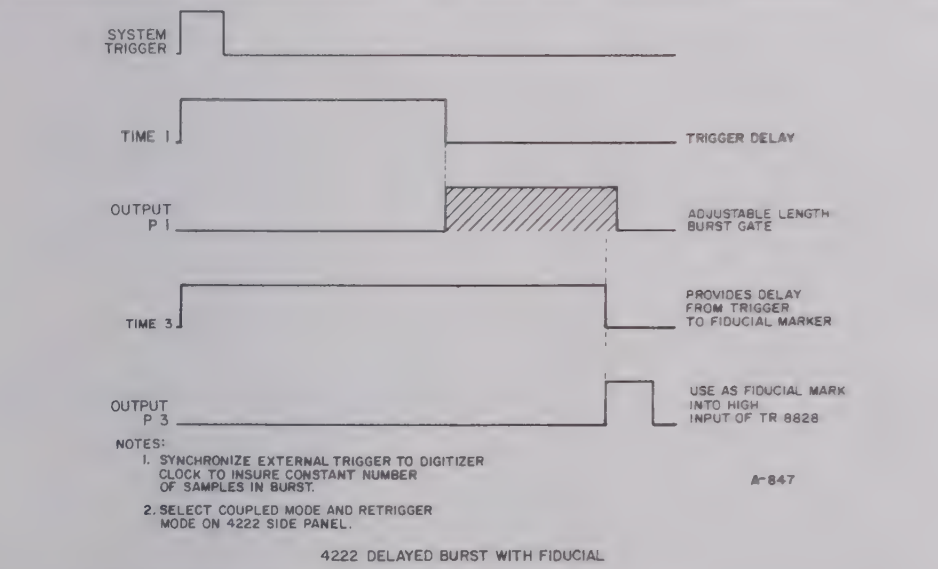


Figure 4.6

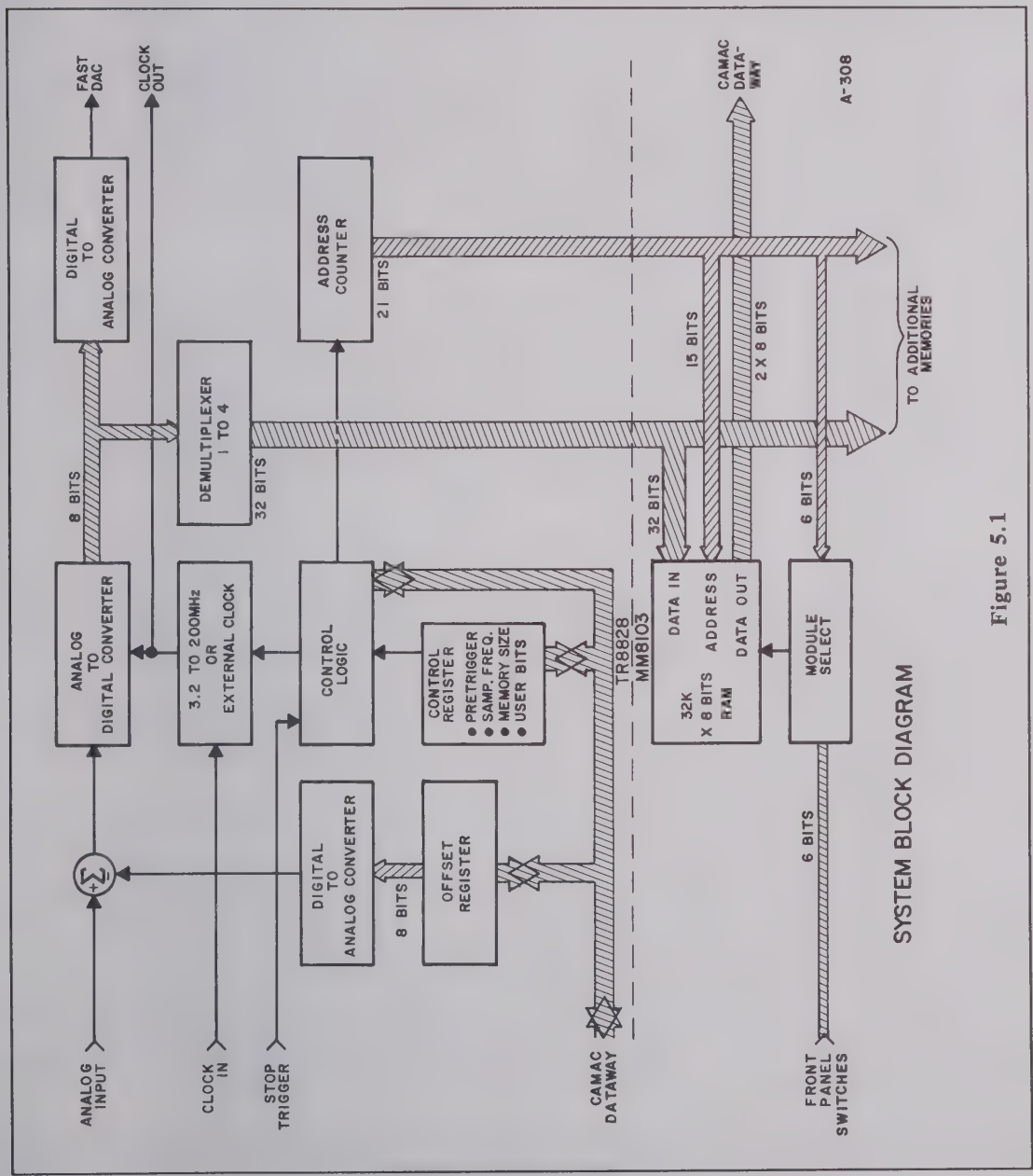

ANALOG INPUT
CLOCK IN
STOP TRIGGER
CAMAC DATAWAY
FRONT PANEL SWITCHES
ANALOG TO DIGITAL CONVERTER
3.2 TO 200MHz OR EXTERNAL CLOCK
CONTROL LOGIC
DIGITAL TO ANALOG CONVERTER
OFFSET REGISTER
CONTROL REGISTER
• PRETRIGGER
• SAMP. FREQ.
• MEMORY SIZE
• USER BITS
TR8828
MM8103
32K X 8 BITS RAM
DATA IN
ADDRESS
DATA OUT
MODULE SELECT
DEMULTIPLEXER 1 TO 4
ADDRESS COUNTER
DIGITAL TO ANALOG CONVERTER
8 BITS
32 BITS
21 BITS
15 BITS
2 X 8 BITS
6 BITS
FAST DAC
CLOCK OUT
CAMAC DATA-WAY
A-308
TO ADDITIONAL MEMORIES
SYSTEM BLOCK DIAGRAM

Figure 5.1

ANALOG-TO-DIGITAL CONVERTER

The Analog-to-Digital Converter (ADC) resides on the left hand circuit board and communicates with the Controller via an internal cable. It transmits data to memory via the front-panel data bus. Critical high-speed analog processing components are all contained in state-of-the-art thick-film hybrid circuits.

In the following description WXX-Y means device W number XX on board Y where Y is R (righthand board) or L (lefthand board). The TR8828C-1 is the lefthand board and the TR8828C-2 is the righthand board.

Analog Processing

Refer to the Schematics and the ADC block diagram in Figure 5.1. Signal inputs are routed via overload protection diodes to U11-L, the track-and-hold. This provides a gain of 5× from the Input and 0.5× from the High Level Input to its output. Also the offset voltage provided by the DAC (U27-R) on the controller card is summed with the input signals. Q2 provides bias current for the output stage of U11-L. U11-L output tracks the input for approximately 2.5 nsec and holds it for the remainder of the clock period.

U11-L output is routed two ways: to the input of U14-L and to U41-L via the analog delay cable mounted on the lefthand side cover. U14-L contains the first rank (coarse) 4-bit ADC and the Digital-to-Analog Converter (DAC). The output of U11-L is applied to U14-L input via a 26.1 Ω series terminator. (The signal line impedance of U14-L is 26 Ω and is internally terminated.) Full scale signal input to U14-L is ±0.64 V, corresponding to ±1.28 V at U11-L output. Adjustable reference voltages for U14-L ADC are provided by U22-L and R79-L; its DAC reference voltage is provided by U4-L, Q1-L and R89-L.

The DAC output of U14-L and the delayed analog signal from U11-L are subtracted and amplified in U41-L, a DC coupled amplifier with subnanosecond risetime. The signal at U41-L output corresponds to the difference between U11-L output and the analog equivalent of the first rank data. It is applied via series terminator R91-L to the second rank (fine) ADC, U54-L, where the second 4-bit conversion takes place. The adjustable reference voltage for U54-L is provided by U65-L and R112-L. R87-L provides adjustment of second rank offset. Q4-L provides bias current for U41-L output stage. U42-L, U55-L, and U57-L are pipeline latches for temporary storage of U14-L data until U54-L data is available.

Digital Processing

The digital processing provides three basic functions: clock generation and selection, byte stacking and byte dropping. Some

sections of the controller circuits reside on the ADC circuit board; this avoids the transmission of clocks and data between ADC and controller at greater than 50 MHz.

The internal clock oscillator consists of Q3–L and Y1–R, a 100 MHz fifth overtone quartz crystal. U17–L converts the clock signal to ECL levels and doubles the clock frequency to 200 MHz. U15–L selects internal or external clock and converts the output of the clock filter back to ECL levels. The clock filter is a pair of coupled tuned circuits designed to eliminate phase jitter due to harmonic or subharmonic components of the clock. U19–L and U27–L buffer and fan out the clock.

Clock pulses to the first and second rank ADC's pipeline latches and clock dividers are generated in the correct phase by high–quality twisted–pair delay cables and differential line receivers. The track–and–hold clock is buffered by U9–L, filtered and phase–shifted by the TR8828C–4 circuit board, and applied to the differential clock inputs of U11–L via an unbalanced–to–balanced transformer, T3–L. R31–L via CR9–L through CR11–L controls the phase and therefore the timing of U11–L clock signal.

The final output of the clock pipeline U19–L is divided by U25–L, U27–L, U29–L to produce the data clock at various sampling rates. U13–L, U20–L and U21–L decode the control signals F4, F5 and F6 which are transmitted via the internal cable from the controller card to select the desired sampling rate or the external clock. U27–L fans the data clock out to the address counter (U35–L), the post–trigger counter (U37–L) and the byte stacker (U59–L, U60–L, U61–L, U62–L). The counters are split between the ADC card and the controller card, thus scaling the 200 MHz sampling clock to 50 MHz before transmitting it to the controller card via the internal cable. AD1 clocks the address counters and PT1 clocks the post–trigger counters on the controller card.

The scalers U35–L and U37–L operate only when the system is writing to memory. When not writing to memory, the data generated by the ADC is ignored. When U33–L and U51–L are set to start the scaling of the address counter, the latch clock to the byte stacker (U66–L, U68–L, U70–L, U72–L, U74–L, U76–L) begins transmitting data via the 50–conductor cable to the memories. The byte stacker accumulates 4 bytes before transmitting them to the memory. Dropping data samples in the byte stacker allows the TR8828C to sample at lower sampling rates.

When a stop command is received, either via the front–panel connector and stop comparator (U53–L) or the CAMAC func-

tion code F(25) and A(0) as decoded by the controller board, the flip flop U46–L is clocked which then enables the post–trigger counter and the clock to the controller card PT1. When the post–trigger samples have been taken, the two LSB's of the address counter are latched by U50–L and saved on the controller card as the start address. Also at this time the write signal to the controller is negated. The address counter and post–trigger counter scalers are then reset and disabled until the next sampling command, F(9) and A(0), is received by the controller.

DIGITAL CONTROLLER

The controller portion of the TR8828C resides on the righthand board and communicates with the ADC board through a 20–conductor cable connecting the two. The controller board is called the TR8828C–2 board. Logic consisting of ECL, CMOS, and TTL is used to minimize power dissipation and maximize performance. ECL is used in the address counter, post–trigger counter, and fast control logic. Registers that are backed up by batteries are CMOS. The rest of the logic is low power Schottky TTL.

CAMAC Control

A(0), N, and NOT F4 are decoded by U34–R. U41–R uses the output of U34–R and the remaining F lines to decode the commands accepted by the TR8828C Series. An X and Q response is generated for all commands by U3–R. Since most commands generate these responses, X and Q are inhibited by those commands that require X=0 and Q=0. Q is inhibited by the inputs to U104–R. X is inhibited by the inputs to U3–R.

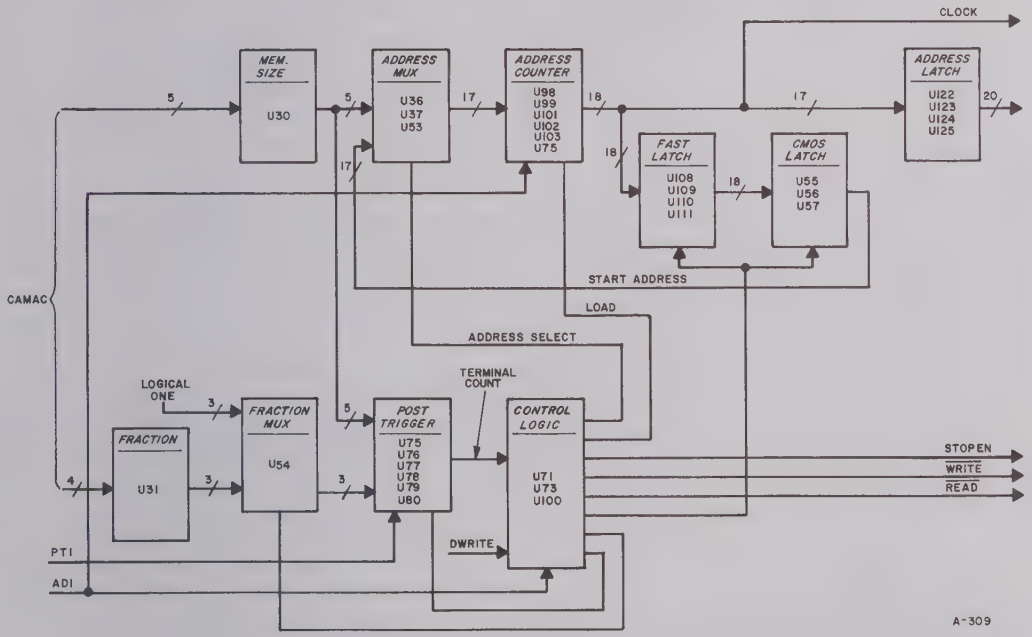
Commands that latch data do so at the time of S1. These commands are AND'd with S1 to produce the appropriate strobes. S2 is used to increment the address counter when reading data so it is AND'd with F(2). F(17) and S2 loads the starting address of the data into the address counter, sets the valid data flip flop, and sets the first byte flip flop. F(9)• S2 set the TR8828C Series into the digitizing or ready state. F(25)•S2 start the post–trigger counter by enabling PT1 on the TR8828C–1 board.

Read commands enable open collector drivers onto the CAMAC read lines. All the registers that can be read by CAMAC must have their signals translated to TTL levels. Low power comparators (LM339s) are used as translators.

Write data from CAMAC is translated to the control registers with LM339 comparators. The registers use –0.8 V and –5.2 V for power with VDD at –0.8 V and VSS at –5.2 V. CMOS can drive ECL logic directly if these supplies are used.

Memory Control

Figure 5.2 is a block diagram of the logic that controls the addressing of memory. The memory is organized as a circular file of data samples. There are two operating modes for the memory control, write to memory and read memory.



Controller Block Diagram
Figure 5.2

Write to memory is initiated by F(9) and A(0). The flip flops U46–L, U51–L are set to wait for the stop. The flip flops U33–L U51–L are set to start the scaling of the address counter and to generate a write to the memory. During the Write mode the 1's complement of the memory size is multiplexed to the data inputs of the address counters. The address counter counts up to terminal count, reloads the 1's complement of the memory size, and proceeds to count up again. Therefore,

memory is loaded with data at addresses starting a full scale – memory size up to an address of full scale –1. This cycle is repeated until a Stop is received.

Stop starts the post–trigger counter. When the write to memory is initiated, F(9) and A(0) loads the post–trigger counter with the 1's complement of the memory size and the fraction or pretrigger size. The post–trigger counter is two counters in series. One (U37–L, U76–R, U77–R, U78–R, U79–R) counts up to the memory size divided by 16 repetitively and the second (U80–R) counts to the fraction multiplied by 16 once. The overall effect is to count the post–trigger samples. At the terminal count of the post–trigger counter, Write is negated. In addition, not Write sets the internal LAM flip flop U95–R. The data can now be read from memory.

Asserting F(17) and A(0) loads the starting address from the CMOS latch into the address counter and loads the memory size and zero pretrigger into the post–trigger counter. Valid Data flip flop U95–R and First Byte flip flop U96–R are also set. The first assertion of F(2) and A(0) will put B0 and B20 onto the R1 and R2 lines of the CAMAC dataway. This is the status word, indicating the position of the start byte in the 2–byte words that are read from memory. The second and successive F(2)s increment the address counter and the post–trigger counter by two. Scaling by two occurs because both flip flops in U75–R are enabled, which enables clocks to the second bit of both counters. The memory modules places 2 bytes onto the read lines of the CAMAC dataway for every read clock. When terminal count is reached in the post–trigger counter, Valid Data is negated and further F(2)s will generate a Q=0 response.

ADC Control

Offset is supplied to the ADC via connector J4. An 8–bit DAC (U27–R) produces a current which flows through a resistor (R15–R) and a potentiometer (R14–R). The resultant voltage is buffered by U20–R. A CMOS register (U29–R) stores the offset value when F(19) and A(0) are asserted. Asserting F(1) and A(0) will enable the stored word via U28–R onto the R9 through R16 lines of the CAMAC dataway.

Power Fail and Battery Backup

Power failure in the controller card is detected by monitoring three of the power supplies used by the card. Zener diodes, resistors, and an opto isolator detect the presences of the ±24 V supplies. A series string of resistors and LED's check the –6 V supply. The result of these checks are AND'd together to produce POWERON. SPF from the ADC and memories is trans-

lated and AND'd with POWERON to enable the X response. Failure of any supply will disable the X response.

Battery backup is accomplished with battery B1–R and diode CR5–R. Resistor R2–R is used to monitor current when the power is off. When a power fail is detected all register clock inputs are held high and tri–state outputs are disabled. Capacitors C15–R, C32–R, and C34–R maintain the logic supplies at their nominal levels while the power fail logic turns everything off.

The –2 V supply is distributed between two regulators and fanned out to the 100 Ω pull–downs with ten individual wires from E11–R through E20–R.

MEMORY MODULES

Refer to Figure 5.3 for a block diagram of the memory design.

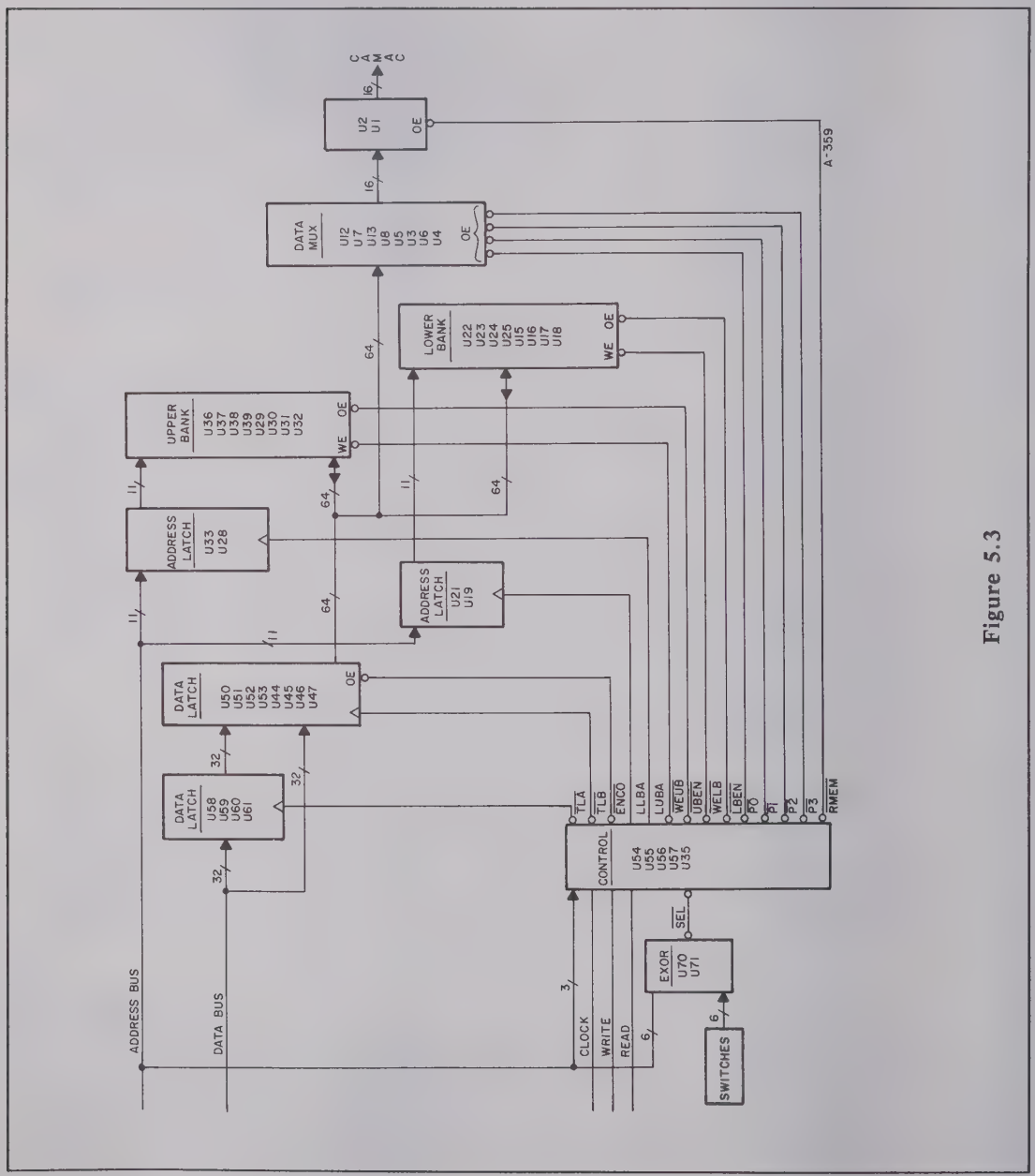
Memory modules contain sixteen 2K × 8 CMOS static ram IC's or sixteen 8K × 8 CMOS static ram IC's for MM8105. Read and write cycle time for these IC's is 120 nsec in MM8103A and MM8105, 70 nsec in MM8104. At the maximum data rate 4 bytes appear at the front panel every 40 nsec. These 4 bytes are assembled into an 8–byte word which is presented simultaneously to an upper bank of eight memory IC's and a lower bank of eight memory IC's. Only one bank gets a write pulse for each 8–byte word. Thus, the worst case minimum cycle time is 160 nsec in MM8103A and MM8105, 80 nsec in MM8104, much slower than the cycle time of the memory IC's.

CAUTION: Unsolder one lead of the battery or remove jumper E1–E2 before attempting repairs on this unit.

Write Cycle

Address and data lines are terminated with removable 100 Ω SIP resistors. The differential clock line is terminated with a single 100 Ω removable resistor. Of the 20 address lines received by the memory the upper six address lines are used as module select lines. These six lines are compared with the front–panel switches to determine whether the module is selected. Exclusive OR's perform this function, generating the signal called SEL which enables appropriate gates in the module.

Both the upper bank and lower bank see their addresses and data inputs from similar sources. This ensures symmetric operation with respect to the address and databus. Address and data latches for both banks accomplish this symmetric operation. Figure 5.4 shows the timing of address, data, and write enable at each memory bank. The data is common to both banks, strobed only at the appropriate time.


CAMAC
16
U2
U1
OE
A-359
DATA MUX
U12
U7
U13
U8
U5
U3
U6
U4
OE
16
LOWER BANK
U22
U23
U24
U25
U15
U16
U17
U18
WE
OE
64
UPPER BANK
U36
U37
U38
U39
U29
U30
U31
U32
WE
OE
64
11
ADDRESS LATCH
U33
U28
11
64
ADDRESS LATCH
U21
U19
11
64
DATA LATCH
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ENCO
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LUBA
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UBEN
WELB
LBEN
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P1
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P3
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U55
U56
U57
U35
3
CLOCK
WRITE
READ
6
SEL
EXOR
U70
U71
6
SWITCHES

Figure 5.3

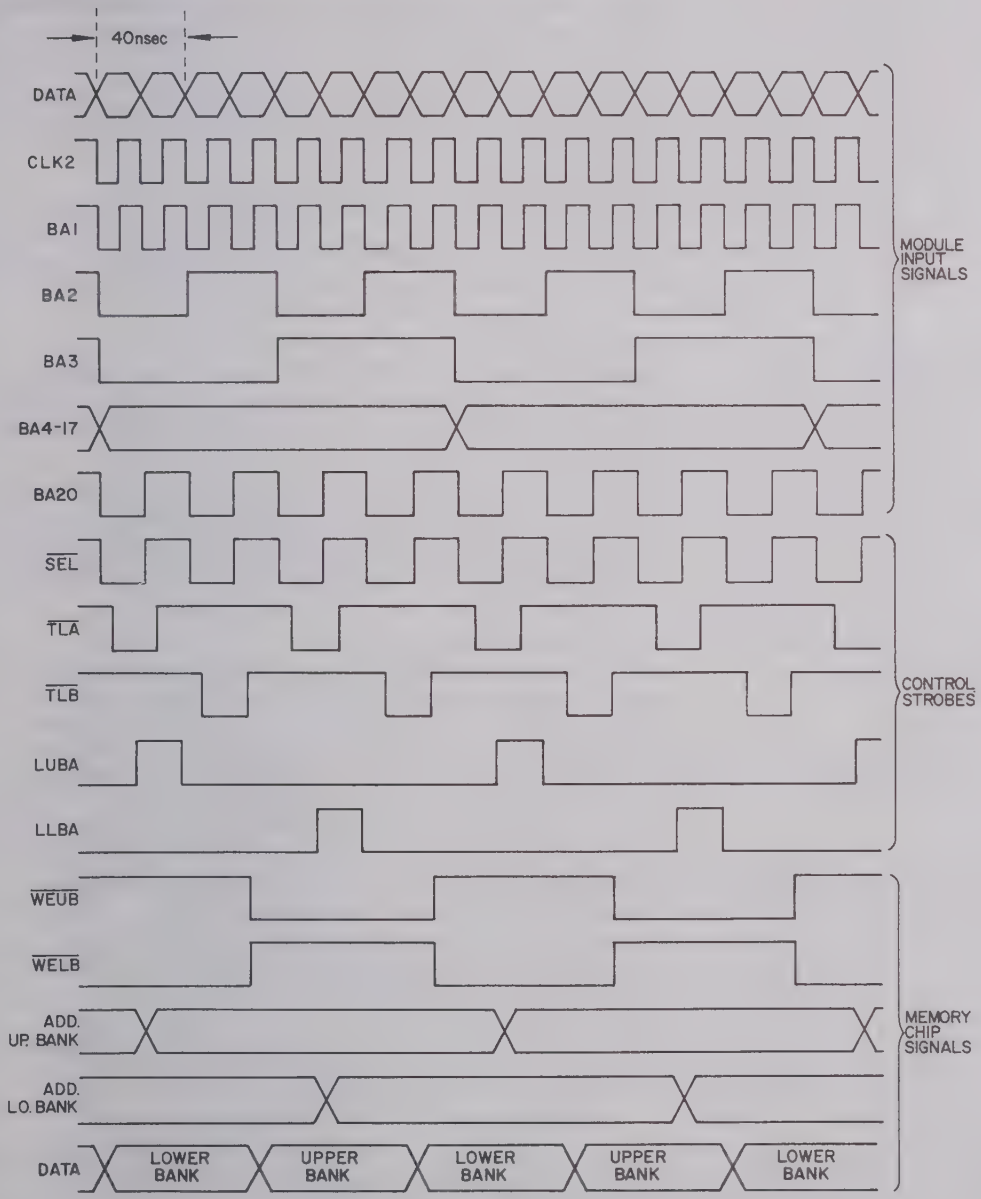
40nsec
DATA
CLK2
BA1
BA2
BA3
BA4-17
BA20
MODULE INPUT SIGNALS
SEL
TLA
TLB
LUBA
LLBA
CONTROL STROBES
WEUB
WELB
ADD. UP. BANK
ADD. LO. BANK
MEMORY CHIP SIGNALS
DATA
LOWER BANK
UPPER BANK
LOWER BANK
UPPER BANK
LOWER BANK

Figure 5.4

Once a write cycle has started, the cycle is completed independent of the state of the SEL line. This is important when more than one module is in a system. As the address bus deselects one module and selects another, the previous write cycle to the last bank must be completed. Write cycles overlap from one module to the next because of pipelining of data within the modules.

Flip flops in U56 control the timing of the write enable pulses to the memory IC's. Clocks are delayed appropriately with gates in U65. Note that signals UBDI and LBDI are not enabled by SEL. This ensures a full-width write enable as long as the clock and address lines continue to toggle.

Read Cycle

During the read cycle AB1, AB2, and AB3 are decoded to read 2 bytes at a time from the 16 memory IC's. Open collector drivers put the bytes onto the R1 through R16 read lines of the CAMAC dataway.

The Read line is simply the decoded F(2) and A(0) from the waveform recorder. The address changes near the end of the CAMAC cycle when S2 increments the address in the waveform recorder. This address change before the end of the Read cycle will create a short enable pulse from the decoders.

Power Fail and Battery Backup

The two power supplies are sensed with a series string of diodes and a resistor. As long as ± 5.2 V is available, the red LED will be enabled and SPF will be low. Loss of power will turn off the red LED and pull SPF to −.08 V. SPF is driven by an open emitter and must have a pull-down in the waveform recorder. On power fail the battery maintains the data in the CMOS memories. Chip select is held high when power is off. Pull-downs to ground on the address lines keep the current requirements of the memory IC's to a minimum during power fail. Resistor R1, in series with the battery, is used to measure the current drain from the battery when the power is off. When the battery is installed, the current is measured to ensure a typical five-year lifetime of the battery.

6 ADDITIONAL INFORMATION

DESCRIPTION OF CAMAC

CAMAC modules may be plugged into a CAMAC mainframe (called Crate in the CAMAC standard) which has up to 25 stations numbered 1 through 25. A station is a slot which accepts a CAMAC module. Some modules occupy several stations. The rightmost two stations are reserved for a Crate Interface or Controller whereas the remainder are Normal Stations used for instrumentation modules. The purpose of the crate controller is to issue CAMAC commands to the modules and transfer information between a computer and the CAMAC modules. It is the interface between the CAMAC Dataway and a computer.

All CAMAC operations take place over the CAMAC Dataway. The Dataway is a parallel bus used to transfer all data, the function coding information, and all status information. In a typical Dataway operation, the crate controller issues a CAMAC command which includes specifying a station number (N), a subaddress (A), and function code (F). In response, the module will generate a valid command accepted (X response) and act on the command. If this command requires data transfer, the read (R) or write (W) lines will be used. Note that the terms Read and Write apply to the crate controller, not the module. For example, under a read command, the crate controller reads data contained within a module.

Whenever there is no Dataway operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look–at–Me line to indicate that it requires attention.

There are also three common control signals made available at all stations:(Z) to Initialize all units, (C) to clear data registers, and (I) to Inhibit (e.g., data–taking).

Definition of CAMAC Commands

The CAMAC command consists of signals on the Dataway lines which specify at least one module (by individual station number lines), a subsection of the module or modules (by the four subaddress bus lines, and the function to be performed (by the five function bus lines). The command signals are maintained for the full duration of the operation on the Dataway.

Station Number

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station.

Subaddress Codes

Different sections of a module are addressed by signals on four A bus lines. These signals are decoded in the module to select one of up to 16 subaddresses, numbered in decimal from A(0) to A(15).

Function Codes

The function to be performed at the specified subaddress in the selected module or modules is defined by the signals on the five F bus lines (F16, F8, F4, F2, F1). These signals are decided in the module to select one of up to 32 functions, numbered in decimal from F(0) to F(31). To see to which functions a particular LeCroy instrument reacts, see its manual.

CAMAC Data

A common parallel highway is used for all data transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines

The crate controller generates data signals on the 24 parallel W bus lines (W1–W24) at the beginning of any Write operation.

The Read Lines

Data signals are set up on the 24 parallel R bus lines (R1–R24) by the instrumentation module as soon as a Read command is recognized. An interface such as the 8901A strobes data from the R bus lines into its own internal registers, whereafter the data is appropriately formatted for GPIB compatible transfers.

Status Information

CAMAC status information is conveyed by signals on the LAM, Busy (B), Response (Q) and Command Accepted (X) lines. This status information is similar to the GPIB service request.

Look–at–Me (LAM)

This, like the N Line, is an individual connection from each station to a separate pin at the control station. When there is no Dataway operation in progress (no B present) any plug–in unit may generate a signal on its L line to indicate that it requires attention, such as is the case when a waveform recorder has finished a conversion sequence. A LAM request can be reset by Clear LAM, Initialize, or by the performance of the specific action which generated the request.

Q Response

The Q busline is used during a Dataway operation to transmit a signal indicating the status of a selected feature of the module, such as whether or not data being read is valid.

Command Accepted

Whenever a module is addressed during a command operation it must generate an X=1 on the Command Accepted busline (X) if it recognizes the command as one that it is equipped to perform.

Command Controls and Signals

The following common control signals operate on all modules within the crate, without requiring address by a command.

Initialize

The initialize signal (Z) has absolute priority over all other signals or controls. It sets all units to a basic state by resetting all registers, and by resetting all LAM signals and disabling them where possible.

Inhibit

The presence of this signal (I) can be used by a module to inhibit any activity (for example, data–taking).

Clear

The common clear signal (C) resets all registers and bistables connected to it.

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SERVICE PROCEDURE

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility.

For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping.

All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned to the Customer Service Department,

a Return Authorization Number is required and may be obtained by contacting the Department at (914) 578-6059 or (914) 425-2000.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, the schematics may not agree in every detail with the accompanying product. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SPARE PARTS

The components used in LeCroy products are referenced on the supplied Replacement Parts List.

Replacement components are available from LeCroy for servicing LeCroy manufactured products. Please contact the Customer Service Department or local field service office and reference the LeCroy 9-digit part number.

PART NUMBER	DESCRIPTION	QUANTITY PER
3828F-1	COMPLETED BOARD TR8828F-1	1
3828F-2	COMPLETED BOARD TR8828F-2	1
3828F-3	COMPLETED BOARD TR8828F-3	1
3828F-4	HARDWARE KIT TR8828F	1
3828F-5	CABLES TR8828F-5	1

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PART NUMBER	DESCRIPTION	QUANTITY PER
2412180	CAP CERA DISC 100V 18 PF	2
2412270	CAP CERA DISC 100V 27 PF	1
2412390	CAP CERA DISC 100V 39 PF	1
3327103	CAP CERA MONO 50V .01 UF	116
3427104	CAP CERA MONO 100V .1 UF	1
2224476	CAP TANT DIP CASE 47 UF	4
2824685	CAP TANT DIP CASE 6.8 UF	48
8849008	CAP VARIABLE 7-40 PF	2
8849010	CAP VARIABLE 1 - 5 PF	1
8879003	CAP VARIABLE 2.5-10 PF	2
8899001	CAP VARIABLE 6-25 PF	3
1225101	RES CARBON FILM 100 OHMS	7
1225102	RES CARBON FILM 1 K	4
1225104	RES CARBON FILM 100 K	5
1225111	RES CARBON FILM 110 OHMS	3
1225151	RES CARBON FILM 150 OHMS	1
1225160	RES CARBON FILM 16 OHMS	1
1225201	RES CARBON FILM 200 OHMS	1
1225202	RES CARBON FILM 2 K	2
1225221	RES CARBON FILM 220 OHMS	1
1225240	RES CARBON FILM 24 OHMS	2
1225271	RES CARBON FILM 270 OHMS	1
1225272	RES CARBON FILM 2.7 K	1
1225301	RES CARBON FILM 300 OHMS	2
1225331	RES CARBON FILM 330 OHMS	2
1225390	RES CARBON FILM 39 OHMS	1
1225470	RES CARBON FILM 47 OHMS	2
1225471	RES CARBON FILM 470 OHMS	9
1225472	RES CARBON FILM 4.7 K	1
1225510	RES CARBON FILM 51 OHMS	6
1225511	RES CARBON FILM 510 OHMS	1
1225560	RES CARBON FILM 56 OHMS	3
1225620	RES CARBON FILM 62 OHMS	14
1225821	RES CARBON FILM 820 OHMS	1
1555510	RES COMP 1W 5% 51 OHMS	1
8531241	RES PREC RN55D 26.1 OHMS	2
8531269	RES PREC RN55D 51.1 OHMS	5
8531281	RES PREC RN55D 68.1 OHMS	1
8531285	RES PREC RN55D 75.0 OHMS	3
8531297	RES PREC RN55D 100 OHMS	2
8531305	RES PREC RN55D 121 OHMS	4
8531325	RES PREC RN55D 196 OHMS	1
8531329	RES PREC RN55D 215 OHMS	1
8531361	RES PREC RN55D 464 OHMS	1
8531369	RES PREC RN55D 562 OHMS	2
8531377	RES PREC RN55D 681 OHMS	1
8531393	RES PREC RN55D 1.00 K	1
8531417	RES PREC RN55D 1.78 K	1
8531422	RES PREC RN55D 2.00 K	2
8531439	RES PREC RN55D 3.01 K	1
8531460	RES PREC RN55D 4.99 K	1
8531469	RES PREC RN55D 6.19 K	1
8531485	RES PREC RN55D 9.09 K	3
8531497	RES PREC RN55D 12.1 K	1

PART NUMBER	DESCRIPTION	QUANTITY PER
8531522	RES PREC RN55D 22.1 K	1
8531569	RES PREC RN55D 68.1 K	1
8531581	RES PREC RN55D 90.9 K	1
0247103	RES VARI CERMET 10 K	1
0247201	RES VARI CERMET 200 OHMS	1
0247202	RES VARI CERMET 2 K	3
0247203	RES VARI CERMET 20 K	1
0247502	RES VARI CERMET 5 K	1
2537501	RES VARI CERMET 500 OHMS	1
0042101	RESISTOR NETWORK 100 OHMS	16
0642560	RESISTOR NETWORK 56 OHMS	2
0330071	IC QUAD 2-IN OR MC14071	2
0340028	IC DECODER MC14028	1
0340210	IC 3-IN 3-OUT OR MC10H210	2
0344102	IC QUAD 2-IN NOR 10H102	1
0344105	IC 2-3-2-IN OR/NOR 10H105	2
0344107	IC 3X 2-IN OR/NOR 10H107	1
0344131	IC DUAL D M-S FLOP 10H131	11
0344176	IC HEX D M-S FLOP 10H176	12
0444016	IC BINARY COUNTER 10H016	1
4042113	IC 4X EXL-OR W/EN F10113P	1
7260768	IC 8-BIT DAC SP9768	1
7444116	IC TRIPL LINE RCVR 10H116	3
8031009	IC VOLT COMPARATOR LM319N	1
8110353	IC DUAL OP AMP LF353N	3
8122337	IC ADJ -VOLT REG LM337T	4
8123002	IC +12 VOLT REG LM340T-12	1
8211002	IC VOLT REF REF-02DP	1
8590806	IC VOLT REG +6V UA7806	1
8620685	IC VOLT COMP SP9685-DG16	1
0110005	DIODE SWITCHING 1N4448	12
5050001	DIODE RECTIFIER 1N4139	3
5050020	DIODE RECTIFIER SSH5A020	1
0225716	DIODE ZENER 12V 1N6002A	5
0513968	DIODE ZENER 20V 5% 1N968B	1
3010835	DIODE HOT CARRIER HP2835	1
4110405	DIODE EPICAP BB405B	4
6030095	DIODE LED RED/GRN CQX-95	1
0020035	OPTICAL ISOLATOR 4N35	2
0170001	TRANSISTOR NPN 2N5770	5
5110001	TRANSISTOR PNP 2N2907A	1
0010001	BEAD SHIELDING FERRITE	9
0050001	CHOKE FERRITE SINGLE LEAD	5
0080001	TOROID CORE (FERRITE)	1
1016221	INDUCTOR MOLDED .22 UH	1
0060125	CRYSTAL .01% 125 MHZ	1
2110003	CONN CO-AXIAL PC MTG SMA	2
2112001	CONN PC MTG LEMO NICKEL	4
3110020	HEADER ASSEMBLY 20-PIN	1
3980002	SHUNT ASSEMBLY 2-POS	7
5760004	SOCKET SINGLE WIRE CLOSED	184
3221004	FUSE PICO II 125V 1 AMP	3
3225001	FUSE PICO II 125V 5 AMP	2
4310003	HDR MALE-MALE 3.2/6.3MM 3	7

PART NUMBER	DESCRIPTION	QUANTITY PER
4313004	HDR SINGL ROW BREAKAWAY 4	2
4610050	HDR DIP SOLDER TO MALE 50	1
8911001	TEST POINT (JACK) WHT	1
0860302	INSULATOR FOR TO-220	6
5212001	HEAT SINK TR8828B-1	2
5449005	WASHER FLAT SIZE #4 NYLON	6
1664030	WIRE BLU SOLID AWG 30	0
1994030	WIRE WHT SOLID AWG 30	0
9010002	HEAT-CONDUCTIVE EPOXY	0
8828221	PC BD PREASS'Y TR8828B-1	1
DAC2	HYB A/D CONVERTER HADAC2	1
DAC3	HYB A/D CONVERTER HADAC3	1
A250A	IC BUFFER AMPLIF HBA250A	1
H201A	IC SAMPLE & HOLD HSH201A	1

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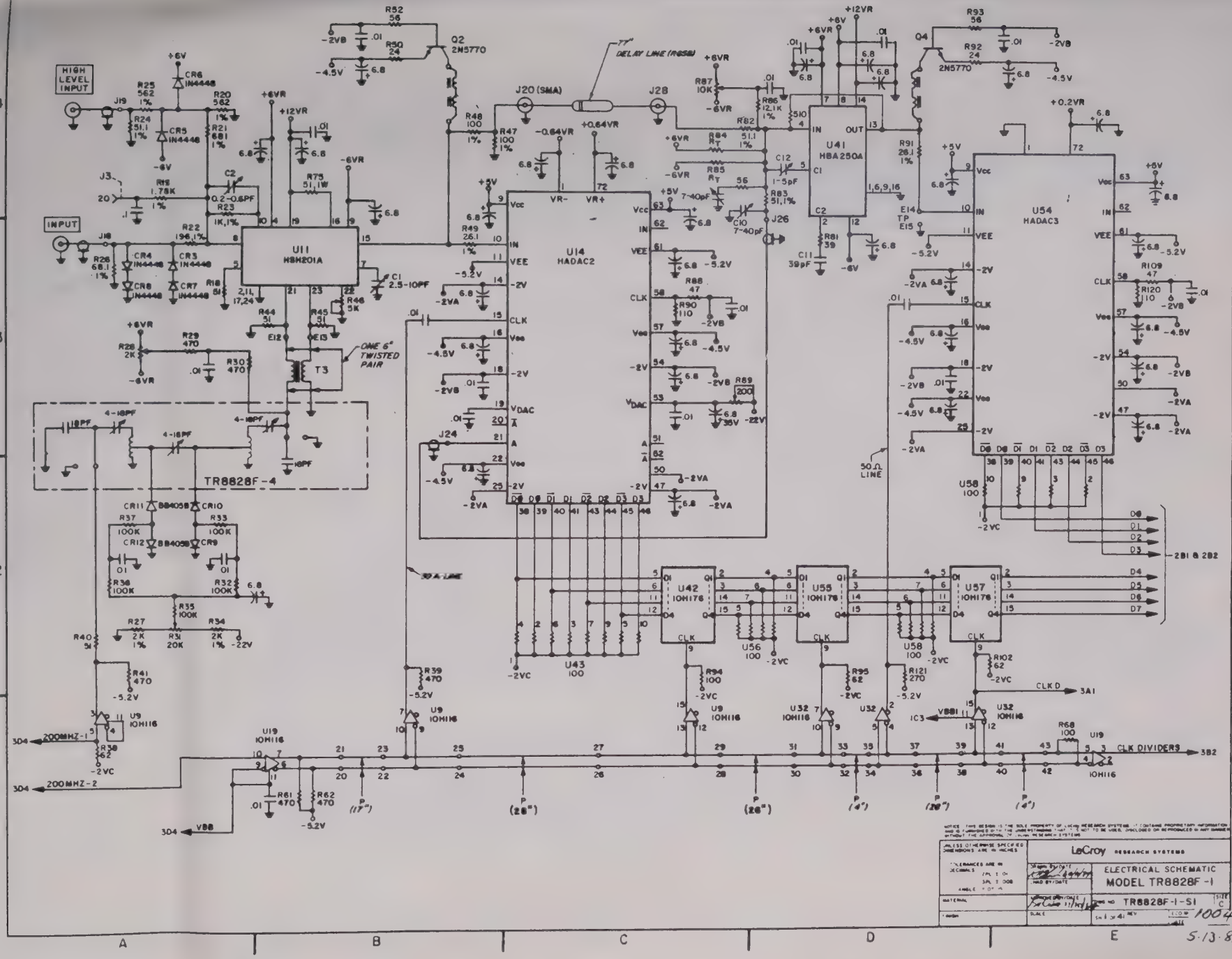
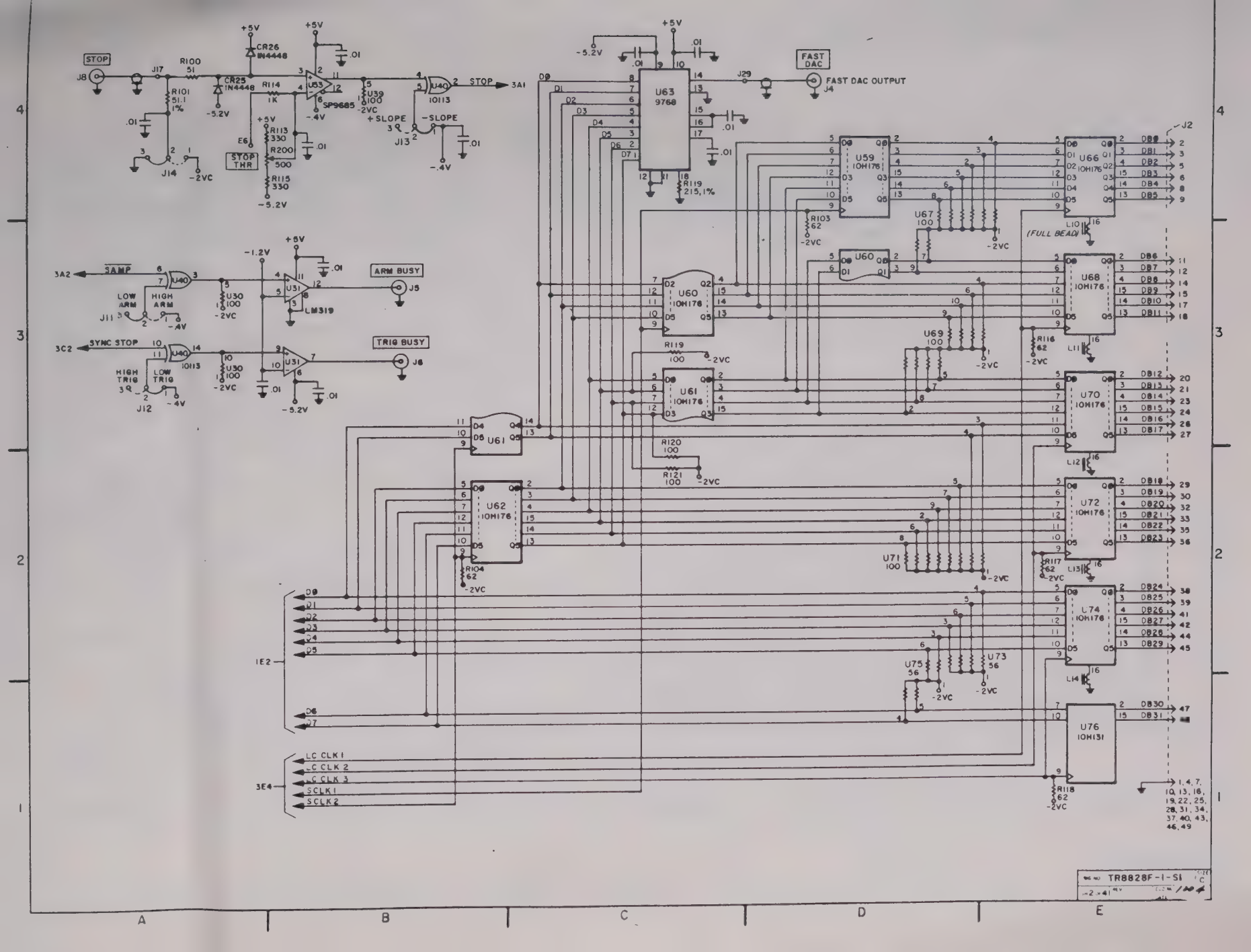
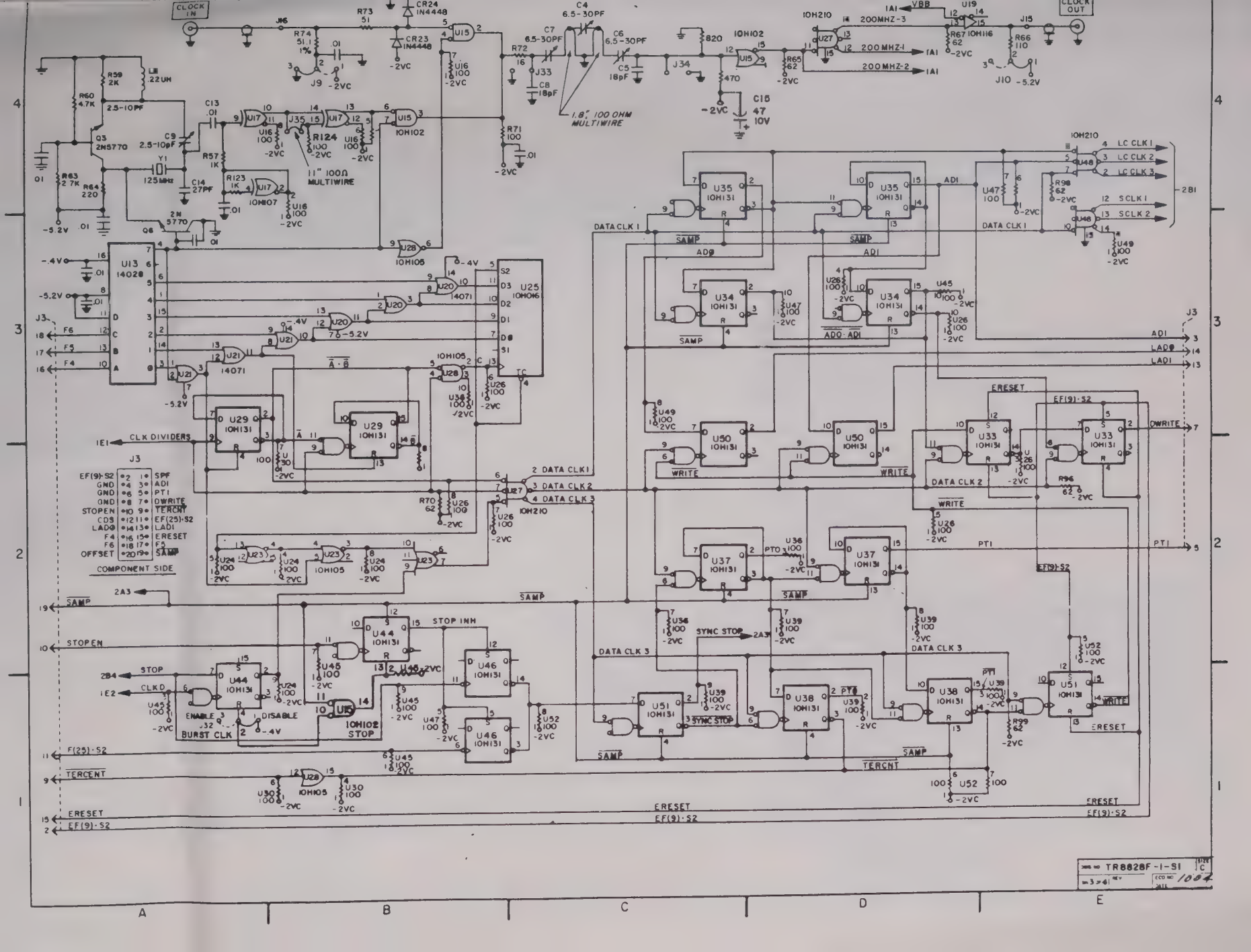
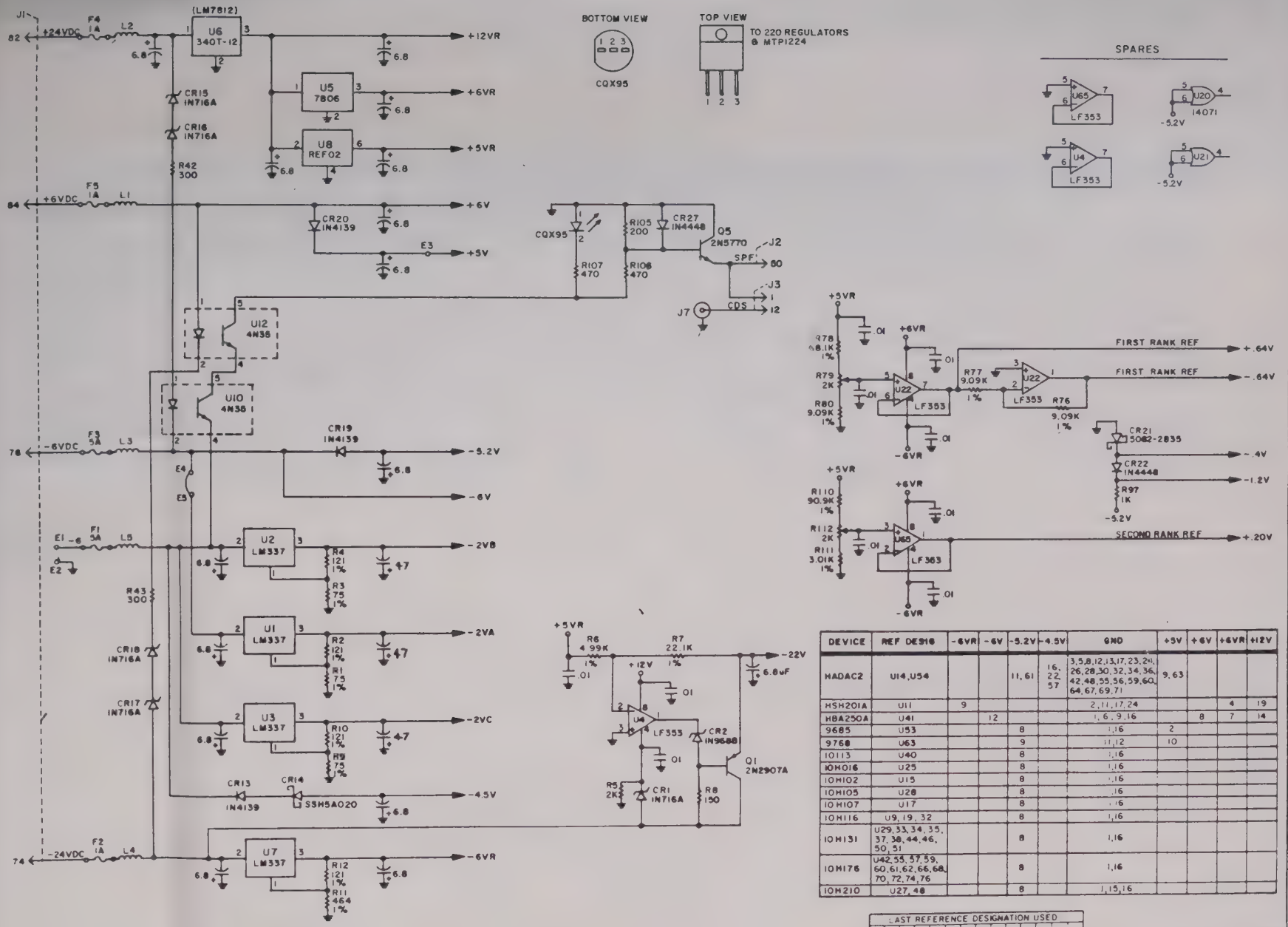

HIGH LEVEL INPUT
INPUT
J19
J18
J3
J20 (SMA)
J28
J26
J24
77" DELAY LINE (RG58)
U11 HSH201A
U14 HADAC2
U41 HBA250A
U54 HADAC3
U42 10H176
U55 10H176
U57 10H176
U43 100
U56 100
U58 100
U9 10H116
U19 10H116
U32 10H116
TR8828F-4
ONE 6" TWISTED PAIR
50Ω LINE
CLK DIVIDERS
200MHZ-1
200MHZ-2
CLK D
LeCroy RESEARCH SYSTEMS
ELECTRICAL SCHEMATIC
MODEL TR8828F-1
TR8828F-1-S1
1004
5-13-85


STOP
J8
J17
R100
51
CR26
IN4448
CR25
IN4448
R101
51.1
1%
-5.2V
R114
1K
U53
SP9685
+5V
-4V
.01
U39
100
-2VC
U40
10113
STOP
3A1
+SLOPE
-SLOPE
J13
-4V
E6
STOP
THR
R113
330
R200
500
R115
330
-5.2V
J14
-2VC
3A2
3AMP
U40
LOW
ARM
HIGH
ARM
J11
U30
100
U31
LM319
-1.2V
ARM BUSY
J5
3C2
SYNC STOP
U40
10113
HIGH
TRIG
LOW
TRIG
J12
U30
100
TRIG BUSY
J6
U63
9760
-5.2V
R119
215,1%
J29
FAST
DAC
FAST DAC OUTPUT
J4
U59
10H176
U60
10H176
U61
10H176
U62
10H176
U66
10H176
U68
10H176
U70
10H176
U72
10H176
U74
10H176
U76
10H131
U67
100
U69
100
U71
100
U73
56
U75
56
R103
62
R116
62
R117
62
R118
62
R104
62
R119
100
R120
100
R121
100
-2VC
L10
L11
L12
L13
L14
(FULL BEAD)
J2
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
DB12
DB13
DB14
DB15
DB16
DB17
DB18
DB19
DB20
DB21
DB22
DB23
DB24
DB25
DB26
DB27
DB28
DB29
DB30
DB31
1E2
3E4
LC CLK 1
LC CLK 2
LC CLK 3
SCLK1
SCLK2
1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31, 34, 37, 40, 43, 46, 49
TR8828F-1-SI


CLOCK IN
CLOCK OUT
J6
J9
J10
J15
R73 51
R74 51.1 1%
CR23 IN4448
CR24 IN4448
U15
U16
R72 16
J33
C7 6.5-30PF
C4 6.5-30PF
C6 6.5-30PF
C8 18pF
C5 18pF
J34
820
470
C15 47 10V
10H102
10H210
U19
U27
R65 62
R67 10H116 62
R66 110
200MHZ-3
200MHZ-1
200MHZ-2
VBB
1A1
-2VC
-5.2V
1.8" 100 OHM MULTIWIRE
R59 2K
L1 .22UH
R60 4.7K
2.5-10PF
Q3 2N5770
C9 2.5-10pF
C13 .01
R57 1K
Y1 125MHz
C14 27PF
R123 1K
10H107
R124 100
11" 100Ω MULTIWIRE
U16 100
R63 2.7K
R64 220
2N 5770
Q6
U28
10H105
U13 14028
U20 14071
U21 14071
U25 10H106
-4V
F6
F5
F4
A·B
U29 10H131
CLK DIVIDERS
IE1
J3
EF(9)-S2
GND
GND
GND
STOPEN
CDS
LADØ
F4
F6
OFFSET
SPF
ADI
PTI
DWRITE
TERCNT
EF(25)-S2
LADI
ERESET
F5
SAMP
COMPONENT SIDE
U24 100
U23
10H105
2 DATA CLK1
3 DATA CLK2
4 DATA CLK3
10H210
R70 62
U26 100
U27
2A3
SAMP
STOPEN
STOP
2B4
CLKD
IE2
U44 10H131
U45 100
U46 10H131
U47 100
U52 100
STOP INH
ENABLE
DISABLE
BURST CLK
10H102
STOP
U32
U35
R124 100
U17
10H107
U30 100
F(25)-S2
TERCNT
ERESET
EF(9)-S2
DATA CLK 1
DATA CLK 2
DATA CLK 3
SAMP
ADØ
ADI
ADØ·ADI
U34 10H131
U35 10H131
U47 100
U48
U49 100
R98 62
LC CLK 1
LC CLK 2
LC CLK 3
SCLK 1
SCLK 2
281
U36 100
U37 10H131
PTØ
PTI
U38 10H131
U39 100
SYNC STOP
2A3
U50 10H131
WRITE
U33 10H131
R96 62
U26 100
U45 100
U51 10H131
R99 62
U52 100
TR8828F-1-SI
REV 3 >41
ECO NO 1004
A
B
C
D
E



DEVICE	REF DESIG	-6VR	-6V	-5.2V	-4.5V	GND	+5V	+6V	+6VR	+12V
HADAC2	U14,U54			11, 61	16, 22, 57	3,5,8,12,13,17,23,24, 26,28,30,32,34,36, 42,48,55,56,59,60, 64,67,69,71	9, 63			
HSH201A	U11	9				2, 11, 17, 24			4	19
HBA250A	U41		12			1, 6, 9, 16		8	7	14
9685	U53			8		1, 16	2			
9768	U63			9		11, 12	10			
10113	U40			8		1, 16				
10H016	U25			8		1, 16				
10H102	U15			8		1, 16				
10H105	U28			8		1, 16				
10H107	U17			8		1, 16				
10H116	U9, 19, 32			8		1, 16				
10H131	U29, 33, 34, 35, 37, 38, 44, 46, 50, 51			8		1, 16				
10H176	U42, 55, 57, 59, 60, 61, 62, 66, 68, 70, 72, 74, 76			8		1, 16				
10H210	U27, 48			8		1, 15, 16				

LAST REFERENCE DESIGNATION USED

NOTE UNLESS OTHERWISE SPECIFIED,
ALL RESISTOR VALUES ARE IN OHMS 1/8W 5%
ALL CAPACITOR VALUES ARE IN MICROFARADS

TR8828F-1-SI

PART NUMBER	DESCRIPTION	QUANTITY PER
2412101	CAP CERA DISC 100V 100PF	2
2412221	CAP CERA DISC 100V 220 PF	1
3326472	CAP CERA MONO 50V 4700 PF	1
3327103	CAP CERA MONO 50V .01 UF	108
3427104	CAP CERA MONO 100V .1 UF	3
2824685	CAP TANT DIP CASE 6.8 UF	11
7214221	CAP ALUM METAL CAN 220 UF	2
1030000	RES COMP ZERO OHMS	1
1225100	RES CARBON FILM 10 OHMS	1
1225102	RES CARBON FILM 1 K	9
1225103	RES CARBON FILM 10 K	5
1225104	RES CARBON FILM 100 K	3
1225106	RES CARBON FILM 10 MEG	1
1225152	RES CARBON FILM 1.5 K	2
1225161	RES CARBON FILM 160 OHMS	1
1225202	RES CARBON FILM 2 K	3
1225331	RES CARBON FILM 330 OHMS	1
1225332	RES COMP 1/8W 5% 3.3 K	1
1225471	RES CARBON FILM 470 OHMS	4
1225512	RES CARBON FILM 5.1 K	1
1225621	RES CARBON FILM 620 OHMS	1
3531305	RES PREC RN55D 121 OHMS	4
3531365	RES PREC RN55D 511 OHMS	1
3531369	RES PREC RN55D 562 OHMS	1
3531422	RES PREC RN55D 2.00 K	1
3531429	RES PREC RN55D 2.37 K	1
3531433	RES PREC RN55D 2.61 K	2
3531445	RES PREC RN55D 3.48 K	1
1467102	RES VARI CERMET 1 K	2
0042101	RESISTOR NETWORK 100 OHMS	9
0042102	RESISTOR NETWORK 1 K	3
0042103	RESISTOR NETWORK 10 K	8
0042222	RESISTOR NETWORK 2.2 K	1
0042471	RESISTOR NETWORK 470 OHMS	2
0832271	RESISTOR NETWORK 270 OHMS	5
0832821	RESISTOR NETWORK 820 OHMS	1
0031028	IC 2-INPUT NAND SN74LS00N	1
0031033	IC 2-INPUT NAND SN7403N	3
0031046	IC HEX INVERTER SN74LS04N	2
0031049	IC D-TYP FLOP SN74LS74N	1
0031051	IC 2-INPUT NOR SN74LS02N	1
0031052	IC 8-INPUT NAND SN74LS30N	3
0031058	IC 2-INPUT AND 7409P	2
0031073	IC 2-IN POS OR SN74LS32N	5
0031075	IC 2-INPUT NAND SN74LS03N	5
0031077	IC 3-INPUT AND SN74LS11N	1
0031086	IC 2-INPUT AND SN74LS08N	1
0041017	IC J-K FLOP SN74LS112N	1
0041044	IC MULTIVIBR SN74LS123N	2
0041062	IC DEC/DEMULTP SN74LS138N	1
0081004	IC DECODER/DEM DM74LS154N	1
0331008	IC 2-IN AND GATE MM74C08N	1
0341109	IC 4-5 IN OR/NOR MC10H109	1
0344102	IC QUAD 2-IN NOR 10H102	2

PART NUMBER	DESCRIPTION	QUANTITY PER
0344105	IC 2-3-2-IN OR/NOR 10H105	3
0444136	IC HEXADEC COUNTR 10H136	1
4022002	IC HEX D M-S F-F MC10176L	8
4042004	IC 2-3-2-IN GATE MC10105P	1
4042007	IC QUAD TRANSL MC10124P	1
4042013	IC HEX COUNTER MC10136P	9
4042103	IC 2-IN OR GATE MC10103P	1
4042135	IC DUAL J-K FLOP MC10135P	2
6023374	IC 8-BIT LATCH MM74C374	6
6033000	IC 2-IN NAND GT MM74C00N	3
6033004	IC HEX INVERTER MM74C04N	1
7172240	IC BUFFER MM74C240	1
7172244	IC LINE DRIVER 74C244	4
7444116	IC TRIPL LINE RCVR 10H116	1
8011007	IC DUAL OP AMP LM358N	1
8031009	IC VOLT COMPARATOR LM319N	1
8031010	IC QUAD DIFF COMP LM339N	15
8041001	IC 8-BIT DAC MONODAC-08EQ	1
8043002	IC 4X FET SWITCH SD5002	2
8122337	IC ADJ -VOLT REG LM337T	2
8123002	IC +12 VOLT REG LM340T-12	1
8124003	IC VOLT REG -12V LM320T-12	1
8211002	IC VOLT REF REF-02DP	1
0110005	DIODE SWITCHING 1N4448	5
5010005	DIODE RECTIFIER 1N4005	1
5050001	DIODE RECTIFIER 1N4139	2
0225720	DIODE ZENER 18V 1N5248	2
3050817	DIODE HOT CARRIER 1N5817	1
6030095	DIODE LED RED/GRN CQX-95	2
6233209	DIODE LED RED MV5075C	3
0020035	OPTICAL ISOLATOR 4N35	2
0170001	TRANSISTOR NPN 2N5770	2
5170002	TRANSISTOR PNP 2N5771	1
0050001	CHOKE FERRITE SINGLE LEAD	4
2660135	BATTERY PC MTG 3 VOLTS	1
0020014	SOCKET IC ST DIP-14	6
3110020	HEADER ASSEMBLY 20-PIN	1
3980002	SHUNT ASSEMBLY 2-POS	1
8063005	W-W PIN, ONE SIDE, 1 WRAP	1
9141008	SWITCH "PIANO DIP" 8-POS	1
3220002	FUSE PICO II 125V 3 AMP	1
3220003	FUSE PICO II 125V .5 AMP	2
3225001	FUSE PICO II 125V 5 AMP	1
4311003	HDR DIP SOLDER TO MALE 3	1
4611034	HDR DIP SOLD TO MALE 34	1
8828222	PC BD PREASS'Y TR8828B-2	1

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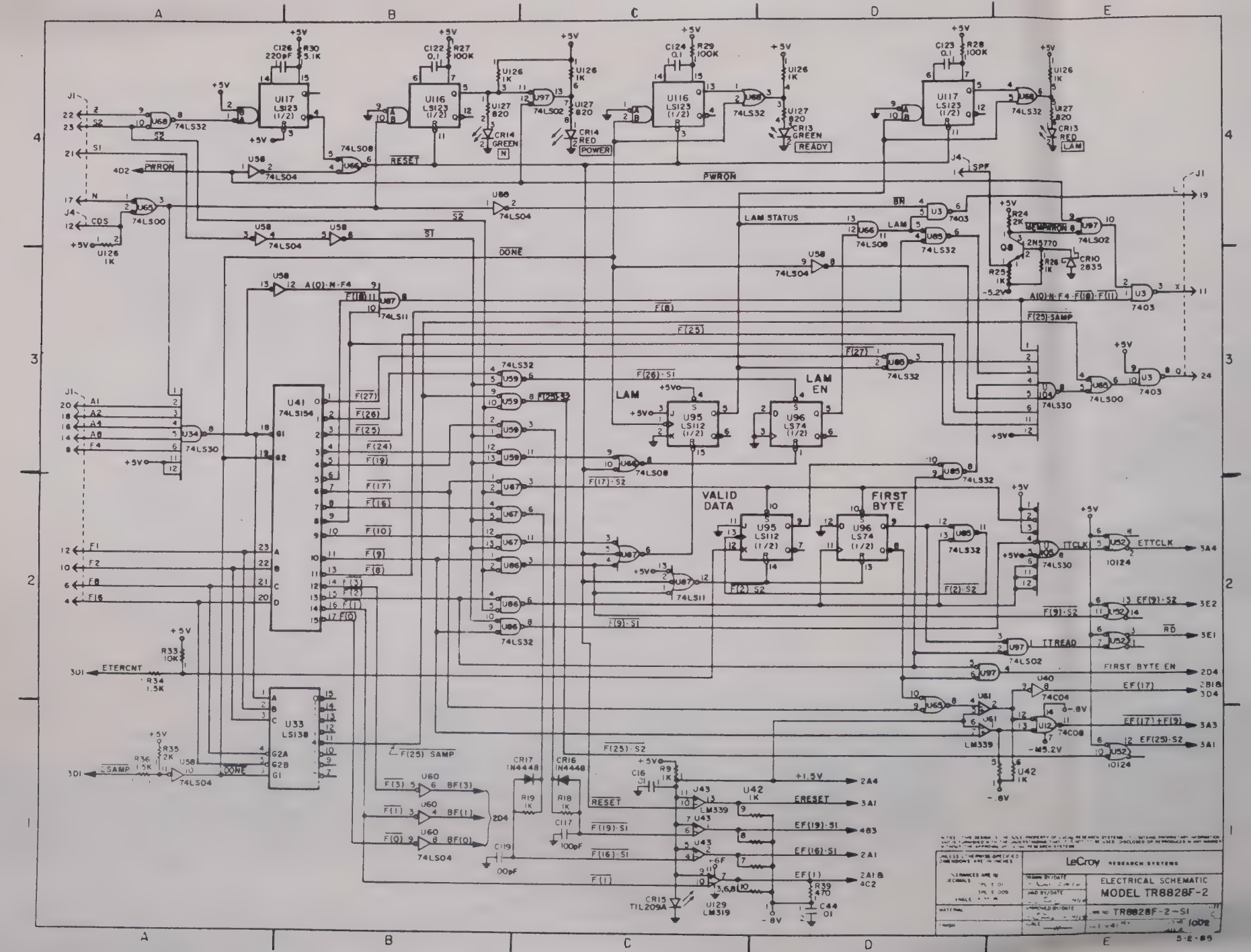
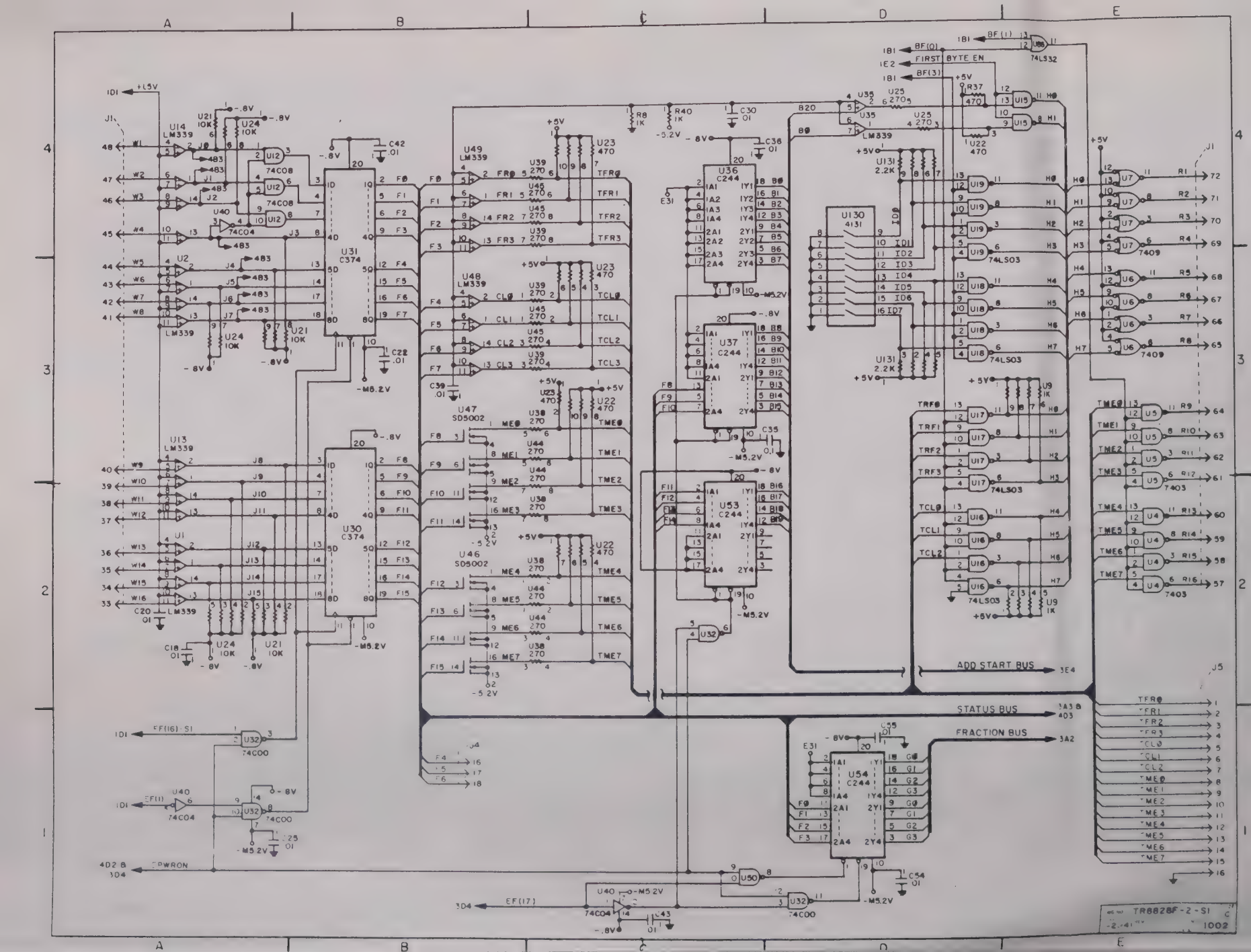
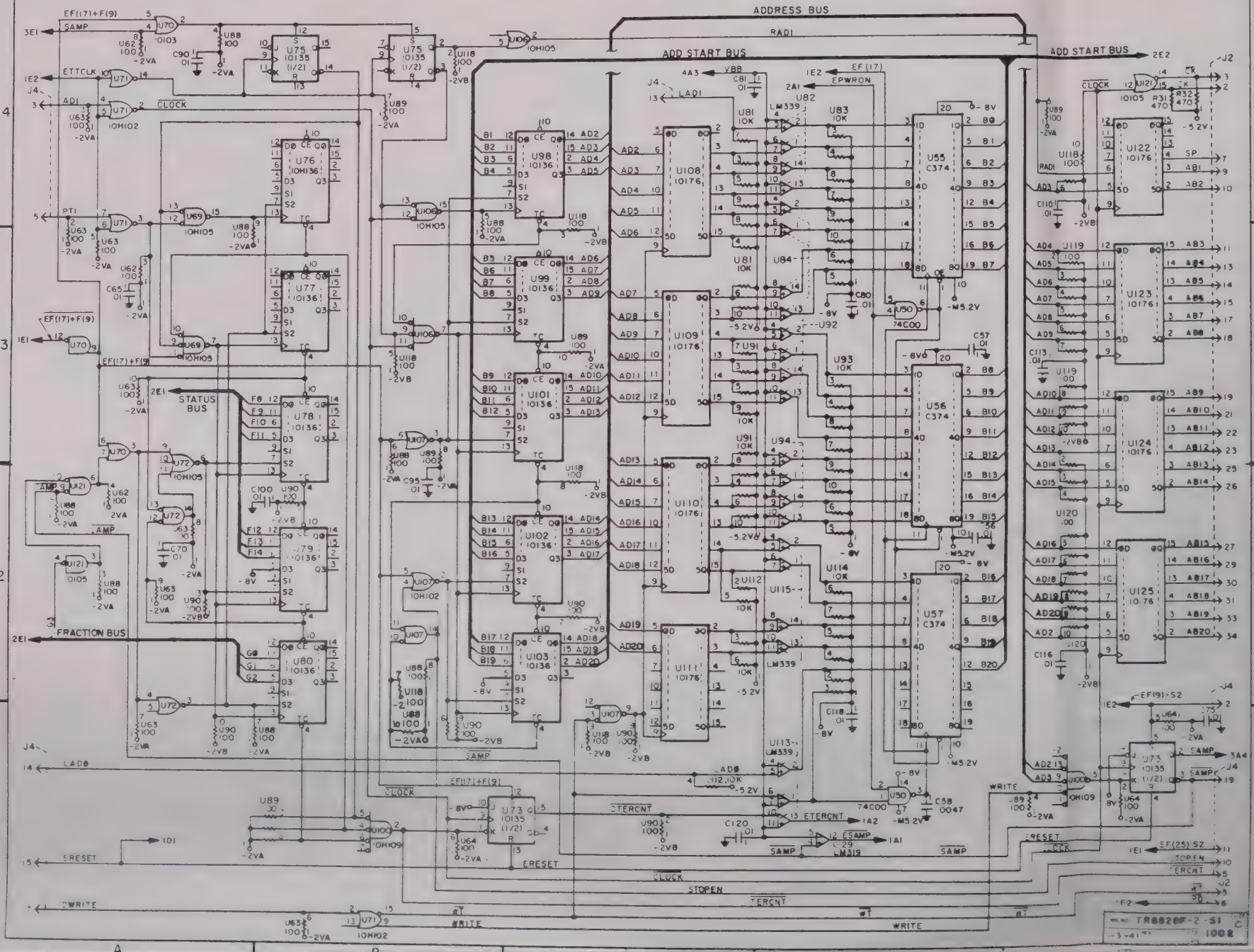
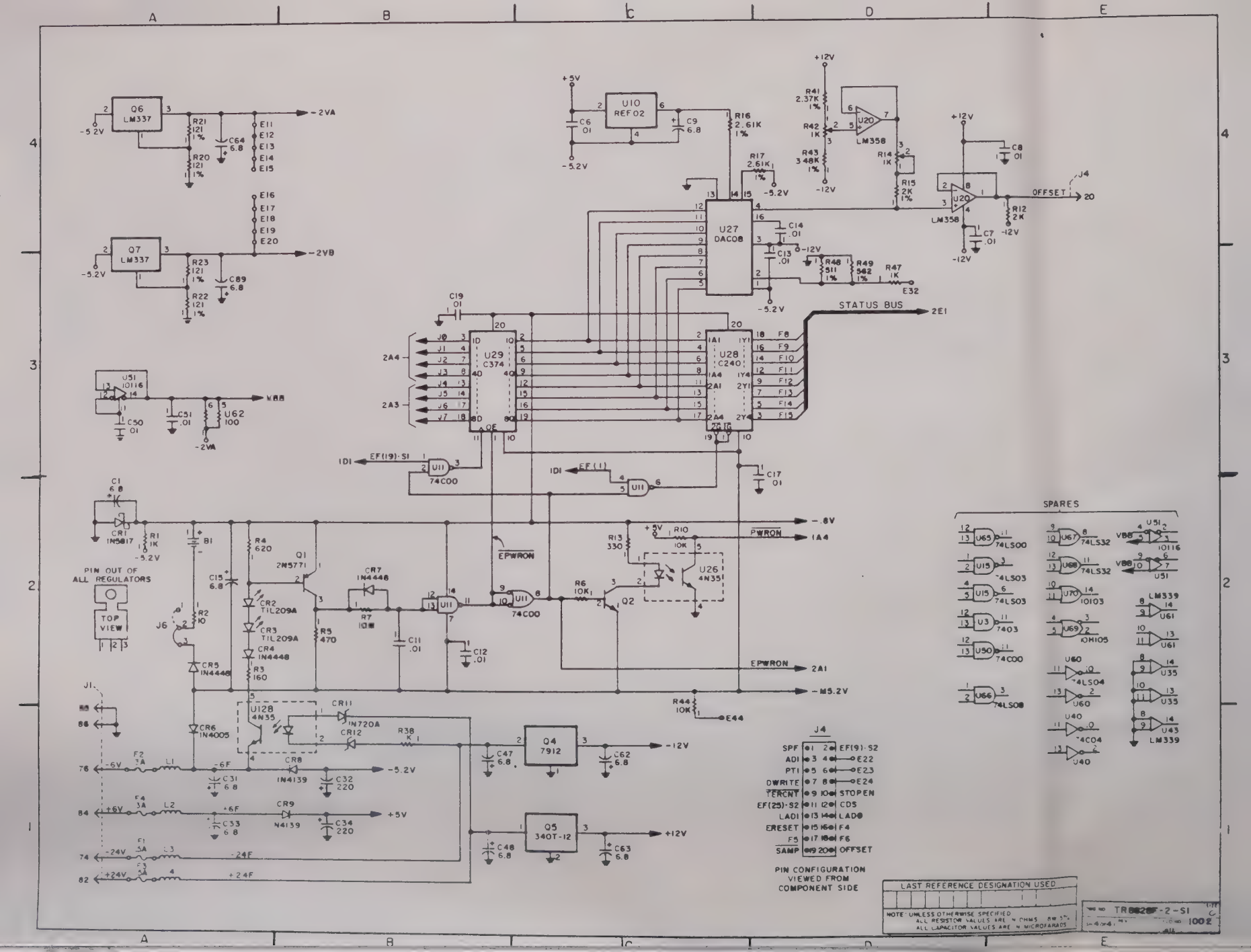

ELECTRICAL SCHEMATIC
MODEL TR8828F-2
LeCroy RESEARCH SYSTEMS
TR8828F-2-SI
5-2-85
LAM
LAM EN
VALID DATA
FIRST BYTE
LAM STATUS
RESET
PWRON
DONE
ETERCNT
FIRST BYTE EN
ITCLK
ITREAD
ERESET
+1.5V
-8V
-5.2V
-M5.2V


+5V
-.8V
-5.2V
-M5.2V
LM339
74C08
74C04
74C00
74LS32
74LS03
7409
7403
U14
U21
U24
U12
U40
U2
U31
C374
U30
U13
U1
U49
U48
U47
SD5002
U46
U23
U22
U39
U45
U38
U44
U36
C244
U37
U53
U54
U130
4131
U131
2.2K
U35
U25
U22
U15
U19
U18
U17
U16
U9
U7
U6
U5
U4
U32
U50
R8
R40
R37
C30
C36
C35
C42
C22
C39
C20
C18
C55
C54
C43
BF(0)
BF(1)
BF(3)
FIRST BYTE EN
ADD START BUS
STATUS BUS
FRACTION BUS
EF(16)-S1
EF(1)
EF(17)
PWRON
TR8828F-2-S1
1002


ADDRESS BUS
RADI
ADD START BUS
ADD START BUS
STATUS BUS
FRACTION BUS
SAMP
CLOCK
ERESET
STOPEN
ETERCNT
WRITE
LADO
EPWRON
TR8920F-2-SI


Q6 LM337
Q7 LM337
R21 121 1%
R20 121 1%
R23 121 1%
R22 121 1%
C64 6.8
C89 6.8
E11
E12
E13
E14
E15
E16
E17
E18
E19
E20
-2VA
-2VB
-5.2V
U10 REF02
C6 .01
C9 6.8
R16 2.61K 1%
R17 2.61K 1%
+5V
+12V
R41 2.37K 1%
R42 1K
R43 348K 1%
U20 LM358
R14 1K
R15 2K 1%
C8 .01
C7 .01
R12 2K
OFFSET
J4
20
U27 DAC08
C14 .01
C13 .01
R48 511 1%
R49 562 1%
R47 1K
E32
STATUS BUS
2E1
U29 C374
U28 C240
C19 .01
2A4
2A3
U51 10116
C50 .01
C51 .01
U62 100
VBB
C17 .01
U11 74C00
EF(19)-S1
EF(1)
1D1
C1 6.8
CR1 1N5817
R1 1K
B1
R4 620
Q1 2N5771
CR2 TIL209A
CR3 TIL209A
CR4 1N4448
R3 160
R5 470
CR5 1N4448
CR6 1N4005
C15 6.8
R2 10
J6
PIN OUT OF ALL REGULATORS
TOP VIEW
J1
B5
B6
CR7 1N4448
R7 10K
C11 .01
C12 .01
EPWRON
R6 10K
Q2
U26 4N35
R13 330
R10 10K
PWRON
1A4
2A1
-8V
-5.2V
R44 10K
E44
U128 4N35
CR11 1N720A
CR12
R38 K1
F2 3A
F4 3A
F1 3A
F3 3A
L1
L2
L3
CR8 1N4139
CR9 N4139
C31 6.8
C32 220
C33 6.8
C34 220
-6V
-6F
+6V
+6F
-24V
-24F
+24V
+24F
-5.2V
+5V
Q4 7912
Q5 340T-12
C47 6.8
C48 6.8
C62 6.8
C63 6.8
-12V
+12V
J4
SPF 1 2 EF(9)-S2
ADI 3 4 E22
PTI 5 6 E23
DWRITE 7 8 E24
TERCNT 9 10 STOPEN
EF(25)-S2 11 12 CDS
LADI 13 14 LADO
ERESET 15 16 F4
F5 17 18 F6
SAMP 19 20 OFFSET
PIN CONFIGURATION VIEWED FROM COMPONENT SIDE
SPARES
U65 74LS00
U15 74LS03
U15 74LS03
U3 7403
U50 74C00
U66 74LS08
U67 74LS32
U68 74LS32
U70 10103
U69 10H105
U60 74LS04
U40 74C04
U51 10116
LM339
U61
U35
U43
LM339
LAST REFERENCE DESIGNATION USED
NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ARE IN OHMS
ALL CAPACITOR VALUES ARE IN MICROFARADS
TR8626F-2-S1
1002

PART NUMBER	DESCRIPTION	QUANTITY PER
18828223	PC BD PREASS'Y TR8828B-3	1

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ART NUMBER	DESCRIPTION	QUANTITY PER
412180	CAP CERA DISC 100V 18 PF	2
879002	CAP VARIABLE 4.0 - 18 PF	3
030000	RES COMP ZERO OHMS	2
060000	CONNECTOR CO-AXIAL BNC	5
313004	HDR SINGL ROW BREAKAWAY 4	2
217701	CABLE CO-AXIAL 77 IN SMA	1
000004	SPACER HEX 2-56X.417	4
256006	SPACER HEX 2-56X3/16	5
440010	SPACER HEX 4-40X5/16	2
203001	SIDE COVER CAMAC STD(LIP)	1
206078	RAIL CAMAC STD TOP W/LIP	3
206178	RAIL CAMAC STD BOT W/LIP	3
209103	REAR PANEL CAMAC SIZE 3	1
430003	CAPTIVE SCREW ASSEMBLY	1
440404	SCREW RND HD NYL 4-40X1/4	4
256005	SCREW PHILIPS 2-56X5/16	4
256002	SCREW FLAT PHIL 2-56X1/8	14
920002	CABLE CO-AXIAL RG 188 A/U	0
857101	PLATE (CABLE) TR8857A	1
828204	PC BD PREASS'Y TR8828-4	1
828222	SIDE CAMAC LEFT TR8828B	1

of report. 21 Details encountered.

PART NUMBER	DESCRIPTION	QUANTITY PER
1597	CAP,CERAMIC DISK 22PF +-COMPOSITE	
1119850	CONN EDAC CE-ED 50-[illegible]	
[illegible]	CONN [illegible] CABLE 34-[illegible] RCPT	
[illegible]	CONNECTOR CABLE 25-SOCKET	
34	[illegible] FOR 24 TO 34-PIN CONN	
50	CAB, FOR [illegible] TO 50-PIN [illegible]	
10	CABLE FLAT AWG 28 [illegible]	
24	CABLE FLAT AWG 28 24-[illegible]	
1010	CABLE [illegible] W/GND 10-COND	

[illegible] parts ordered.

PART NUMBER	DESCRIPTION	QUANTITY PER
7161637	LABEL BLANK YEL -COMPUTER	2
3211050	CONN FLAT CABLE 50-POS	2
3220034	CONN FLAT CABLE 34-SOCKET	2
3260020	CONN FLAT CABLE 20-SOCKET	2
3910034	TAB FOR 24 TO 34-PIN CONN	3
3910050	TAB FOR 28 TO 50-PIN CONN	3
2030020	CABLE FLAT AWG 28 20-COND	0
2030034	CABLE FLAT AWG 28 34-COND	0
2040050	CABLE FLAT W/GND 50-COND	0

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